PATENT ABSTRACTS OF JAPAN

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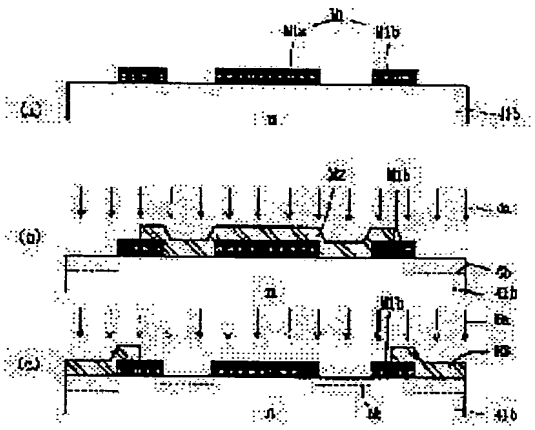
(54) MANUFACTURE OF VERTICAL SILICON CARBIDE FET AND VERTICAL SILICON CARBIDE FET

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a very precise channel having a high breakdown strength by forming each impurity introducing area in a self-aligning way, by specifying each impurity introducing area with the partial end and the other part of one mask of a plurality of masks by using another mask partially overlapping the mask.



SOLUTION: After a polycrystalline silicon film is deposited on the surface of an n-type drift layer 41b, a mask M1 is formed by patterning this silicon film. The mask M1 is composed of a central section M1a and both side sections M1b. Then, after an SiO2 film is deposited on the mask M1 and a mask M2 is formed by patterning the SiO2 film, source regions are formed by implanting ions 4a which become an n-type impurity into the regions regulated by the masks M1 and M2. The mask M2 can be easily aligned with the mask M1, because no further alignment is required when the end of the mask M2 is on the mask M1. After the mask M2 is removed and a mask M3 is formed by again forming a pattern, p-type gate region is formed by injecting ions 5a which becomes a p-type impurity into the region regulated by the masks M1 and M3.

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29/808		29/78	６５２Ｔ
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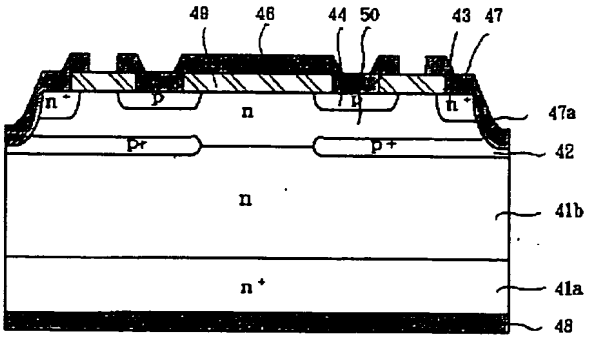
(54)【発明の名称】　炭化けい素縦形ＦＥＴの製造方法および炭化けい素縦形ＦＥＴ

(57)【要約】

【課題】非常に精密で均一なチャネルが実現でき、かつ容易に高耐圧できるＳｉＣを用いた縦形のＦＥＴの製造方法を提供する。

【解決手段】第一のマスクと一部重複する第二のマスクとを用いて第一のマスクの一部の一方の端により第一導電型不純物導入領域を規定し、第一のマスクの一部および第二のマスクを除去して第一のマスクの別の部分により第二導電型不純物導入領域を規定することによって、第一導電型不純物導入領域および第二導電型不純物導入領域を自己整合的に形成する。また、端部をテーパー状にしたマスクを用い、加速電圧を変えてイオン注入する方法を取れば、一枚のマスクだけで、第一導電型不純物導入領域および第二導電型不純物導入領域を自己整合的に形成する。特に、チャネル領域の不純物濃度を制御することによって、しきい電圧を制御することができ、また、ノーマリオフのＦＥＴとすることができる。



41a　n⁺ ドレイン層
41b　ｎドリフト層
42　ｐ⁺ 埋め込み領域
43　n⁺ ソース領域
44　ｐゲート領域
46　ゲート電極
47　ソース電極
47a　凹部
48　ドレイン電極
49　絶縁膜
50　ｎチャネル領域

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【特許請求の範囲】

【請求項１】第一導電型炭化けい素サブストレート上に積層された炭化けい素からなる第一導電型ドリフト層と、その第一導電型ドリフト層の表面層に選択的に互いに隔離して形成された第二導電型ゲート領域、第一導電型ソース領域と、その第二導電型ゲート領域および第一導電型ソース領域の下方に選択的に形成された第二導電型埋め込み領域と、第二導電型ゲート領域の表面に接触して設けられたゲート電極層と、第一導電型ソース領域と第二導電型埋め込み領域との表面に共通に接触して設けられたソース電極と、炭化けい素サブストレートの裏面に設けられたドレイン電極とを有する縦形ＦＥＴの製造方法において、第一のマスクの一部の一方の端により第一導電型ソース領域の一方の端を規定し、第一のマスクの一部の他方の端と第一のマスクの他の部分とにより第二導電型ゲート領域を規定し、前記第一のマスクの他の部分により第二導電型埋め込み領域の端を規定してそれぞれの領域を形成することを特徴とする炭化けい素縦形ＦＥＴの製造方法。

【請求項２】第一導電型炭化けい素サブストレート上に炭化けい素からなる第一導電型ドリフト層がエピタキシャル成長により積層された基板を用い、その第一導電型ドリフト層の表面上に第一のマスクを形成する工程と、第一のマスクと一部が重複するように第一のマスクとは異なる材料からなる第二のマスクを形成する工程と、それらのマスクにより選択的に第一導電型ドリフト層の表面層に第一導電型ソース領域形成のための不純物を導入する工程と、第二のマスクを除去する工程と、第一のマスクと一部が重複するように第一のマスクとは異なる材料からなる第三のマスクを形成する工程と、それらのマスクにより選択的に第一導電型ドリフト層の表面層に第二導電型ゲート領域形成のための不純物を導入する工程と、第一のマスクの一部を残して第一のマスク、第三のマスクを除去する工程と、そのマスクにより選択的に第一導電型ドリフト層の表面層に第二導電型埋め込み領域形成のための不純物を導入する工程と、導入した不純物を活性化するための熱処理工程と、炭化けい素基板表面に第四のマスクを形成する工程と、そのマスクにより第一導電型ソース領域の表面から第二導電型埋め込み領域に達する凹部を形成する工程と、絶縁物からなる第五のマスクを形成する工程と、金属膜を蒸着する工程と、その金属膜からなるゲート電極、ソース電極、ドレイン電極を形成する工程とからなる炭化けい素縦形ＦＥＴの製造方法。

【請求項３】第一導電型炭化けい素サブストレート上に炭化けい素からなる第一導電型ドリフト層がエピタキシャル成長により積層された基板を用い、その第一導電型ドリフト層の表面上に第一のマスクを形成する工程と、第一のマスクと一部が重複するように第一のマスクとは異なる材料からなる第二のマスクを形成する工程と、そ

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れらのマスクにより選択的に第一導電型ドリフト層の表面層に第一導電型ソース領域形成のための不純物を導入する工程と、第二のマスクを除去する工程と、第一のマスクと一部が重複するように第一のマスクとは異なる材料からなる第三のマスクを形成する工程と、それらのマスクにより選択的に第一導電型ドリフト層の表面層に第二導電型ゲート領域形成のための不純物を導入する工程と、第一のマスクの一部を残して第一のマスク、第三のマスクを除去する工程と、そのマスクにより選択的に第一導電型ドリフト層の表面層に第二導電型埋め込み領域形成のための不純物を導入する工程と、炭化けい素基板表面に第四のマスクを形成する工程と、そのマスクにより第二導電型コンタクト領域形成のための不純物を導入する工程と、導入した不純物を活性化するための熱処理工程と、絶縁物からなる第五のマスクを形成する工程と、金属膜を蒸着する工程と、その金属膜からなるゲート電極、ソース電極、ドレイン電極を形成する工程とからなる炭化けい素縦形ＦＥＴの製造方法。

【請求項４】第一導電型ソース領域、第二導電型ゲート領域、第二導電型埋め込み領域形成のための不純物の導入がいずれもイオン注入によっておこなわれることを特徴とする請求項２または３に記載の炭化けい素縦形ＦＥＴの製造方法。

【請求項５】第一導電型ドリフト層の表面とショットキー接合を形成する電極を設けることを特徴とする請求項１ないし４のいずれかに記載の炭化けい素縦形ＦＥＴの製造方法。

【請求項６】第一導電型炭化けい素サブストレート上に積層された炭化けい素からなる第一導電型ドリフト層と、その第一導電型ドリフト層の表面層に選択的に形成された第一導電型ソース領域と、第一導電型ソース領域の下方に選択的に形成された第二導電型埋め込み領域と、第一導電型ドリフト層の表面上にゲート絶縁膜を介して設けられたゲート電極層と、第一導電型ソース領域と第二導電型埋め込み領域との表面に共通に接触して設けられたソース電極と、炭化けい素サブストレートの裏面に設けられたドレイン電極とを有する縦形ＦＥＴの製造方法において、第一のマスクの一部により第一導電型ソース領域の一方の端を規定し、前記第一のマスクの他の部分により第二導電型埋め込み領域の端を規定することを特徴とする炭化けい素縦形ＦＥＴの製造方法。

【請求項７】第一導電型炭化けい素サブストレート上に炭化けい素からなる第一導電型ドリフト層がエピタキシャル成長により積層された基板を用い、その第一導電型ドリフト層の表面上に第一のマスクを形成する工程と、第一のマスクと一部が重複するように第一のマスクとは異なる材料からなる第二のマスクを形成する工程と、それらのマスクにより選択的に第一導電型ドリフト層の表面層に第一導電型ソース領域形成のための不純物を導入

する工程と、第一のマスクの一部を残して第一のマスク、第二のマスクを除去する工程と、それらのマスクにより選択的に第一導電型ドリフト層の表面層に第二導電型埋め込み領域形成のための不純物を導入する工程と、残した第一のマスクの一部を除去する工程と、導入した不純物を活性化するための熱処理工程と、炭化けい素基板表面に熱酸化によりゲート酸化膜を形成する工程と、そのゲート酸化膜上に多結晶シリコン層を堆積した後パターン形成する工程と、絶縁膜を被覆した後第三のマスクを形成する工程と、そのマスクにより第一導電型ソース領域の表面から第二導電型埋め込み領域に達する凹部を形成する工程と、絶縁膜に接触用の窓を設け金属膜を蒸着する工程と、その金属膜からなり多結晶シリコン層に接触するゲート電極、第一導電型ソース領域と第二導電型コンタクト領域とに接触するソース電極、炭化けい素サブストレートに接触するドレイン電極を形成する工程とからなる炭化けい素縦形ＦＥＴの製造方法。

【請求項８】第一導電型炭化けい素サブストレート上に炭化けい素からなる第一導電型ドリフト層がエピタキシャル成長により積層された基板を用い、その第一導電型ドリフト層の表面上に第一のマスクを形成する工程と、第一のマスクと一部が重複するように第一のマスクとは異なる材料からなる第二のマスクを形成する工程と、それらのマスクにより選択的に第一導電型ドリフト層の表面層に第一導電型ソース領域形成のための不純物を導入する工程と、第一のマスクの一部を残して第一のマスク、第二のマスクを除去する工程と、それらのマスクにより選択的に第一導電型ドリフト層の表面層に第二導電型埋め込み領域形成のための不純物を導入する工程と、炭化けい素基板表面に第三のマスクを形成する工程と、そのマスクにより第二導電型埋め込み領域に達する第二導電型コンタクト領域形成のための不純物を導入する工程と、導入した不純物を活性化するための熱処理工程と、炭化けい素基板表面に熱酸化によりゲート酸化膜を形成する工程と、そのゲート酸化膜上に多結晶シリコン層を堆積した後パターン形成する工程と、絶縁膜を被覆する工程と、その絶縁膜に接触用の窓を設け金属膜を蒸着する工程と、その金属膜からなり多結晶シリコン層に接触するゲート電極、第一導電型ソース領域と第二導電型コンタクト領域とに接触するソース電極、炭化けい素サブストレートに接触するドレイン電極を形成する工程とからなる炭化けい素縦形ＦＥＴの製造方法。

【請求項９】第一導電型炭化けい素サブストレート上に積層された炭化けい素からなる第一導電型ドリフト層と、その第一導電型ドリフト層の表面層に選択的に形成された第一導電型ソース領域と、第一導電型ソース領域の下方に選択的に形成された第二導電型ベース領域と、第一導電型ドリフト層の表面上にゲート絶縁膜を介して設けられたゲート電極層と、第一導電型ソース領域と第二導電型ベース領域との表面に共通に接触して設けられ

たソース電極と、炭化けい素サブストレートの裏面に設けられたドレイン電極とを有する縦形ＦＥＴの製造方法において、端部がゆるやかなテーパー状の第一のマスクの厚さの厚い部分により第一導電型ソース領域の一方の端を規定し、前記第一のマスクの第一のマスクの厚さの薄い部分により第二導電型ベース領域の端を規定することを特徴とする炭化けい素縦形ＦＥＴの製造方法。

【請求項１０】第一導電型炭化けい素サブストレート上に炭化けい素からなる第一導電型ドリフト層がエピタキシャル成長により積層された基板を用い、その第一導電型ドリフト層の表面上に端部がゆるやかなテーパー状の第一のマスクを形成する工程と、そのマスクの厚さの厚い部分により選択的に第一導電型ドリフト層の表面層に第二導電型ベース領域形成のための不純物を導入する工程と、第一のマスクの厚さの薄い部分により選択的に第一導電型ドリフト層の表面層に第一導電型ソース領域形成のための不純物を導入する工程と、炭化けい素基板表面に第三のマスクを形成する工程と、そのマスクにより第二導電型ベース領域に達する第二導電型コンタクト領域形成のための不純物を導入する工程と、導入した不純物を活性化するための熱処理工程と、炭化けい素基板表面に熱酸化によりゲート酸化膜を形成する工程と、そのゲート酸化膜上に多結晶シリコン層を堆積した後パターン形成する工程と、絶縁膜を被覆した後接触用の窓を設け金属膜を蒸着する工程と、その金属膜からなり多結晶シリコン層に接触するゲート電極、第一導電型ソース領域と第二導電型コンタクト領域とに接触するソース電極、炭化けい素サブストレートに接触するドレイン電極を形成する工程とからなる炭化けい素縦形ＦＥＴの製造方法。

【請求項１１】第一導電型炭化けい素サブストレート上に炭化けい素からなる第一導電型ドリフト層がエピタキシャル成長により積層された基板を用い、その第一導電型ドリフト層の表面上に端部がゆるやかなテーパー状の第一のマスクを形成する工程と、そのマスクの厚さの厚い部分により選択的に第一導電型ドリフト層の表面層に第一導電型ソース領域形成のための不純物を導入する工程と、第一のマスクの厚さの厚い部分により選択的に第一導電型ドリフト層の表面層に第二導電型ベース領域形成のための不純物を導入する工程と、炭化けい素基板表面に第三のマスクを形成する工程と、そのマスクにより第二導電型ベース領域に達する第二導電型コンタクト領域形成のための不純物を導入する工程と、第一のマスクを除去する工程と、導入した不純物を活性化するための熱処理工程と、炭化けい素基板表面に熱酸化によりゲート酸化膜を形成する工程と、そのゲート酸化膜上に多結晶シリコン層を堆積した後パターン形成する工程と、絶縁膜を被覆した後第三のマスクを形成する工程と、そのマスクにより第一導電型ソース領域の表面から第二導電型コンタクト領域に達する凹部を形成する工程と、絶縁

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膜に接触用の窓を設け金属膜を蒸着する工程と、その金属膜からなり多結晶シリコン層に接触するゲート電極、第一導電型ソース領域と第二導電型コンタクト領域とに接触するソース電極、炭化けい素サブストレートに接触するドレイン電極を形成する工程とからなる炭化けい素縦形ＦＥＴの製造方法。

【請求項１２】第一のマスクの側方にサイドウォールを設け、第一のマスクとそのサイドウォールとを第三のマスクとすることを特徴とする請求項１０または１１に記載の炭化けい素縦形ＦＥＴの製造方法。

【請求項１３】第二導電型ベース領域に達する第二導電型コンタクト領域形成のための厚さの厚い第三のマスクを形成する工程と、そのマスクにより不純物を導入する工程を先に経た後、その第三のマスクをエッチバックして端部がゆるやかなテーパー状の第一のマスクとすることを特徴とする請求項９ないし１１のいずれかに記載の炭化けい素縦形ＦＥＴの製造方法。

【請求項１４】第一導電型ソース領域、第二導電型埋め込み領域、第二導電型ベース領域形成のための不純物の導入がいずれもイオン注入によっておこなわれることを特徴とする請求項６ないし１３のいずれかに記載の炭化けい素縦形ＦＥＴの製造方法。

【請求項１５】第一導電型ドリフト層の表面層の全面にチャネル領域の不純物濃度制御のための第一導電型不純物を導入する工程が加えられていることを特徴とする請求項１ないし１４のいずれかに記載の炭化けい素縦形ＦＥＴの製造方法。

【請求項１６】第一導電型炭化けい素サブストレート上に積層された炭化けい素からなる第一導電型ドリフト層と、その第一導電型ドリフト層の表面層に選択的に少なくとも一部が埋め込まれて形成された第二導電型ベース領域と、その第二導電型ベース領域の上方の一部に第二導電型ベース領域と接して形成された第一導電型ソース領域と、第二導電型ベース領域上に残された第一導電型ドリフト層であるチャネル領域上にゲート絶縁膜を介して設けられたゲート電極層と、第一導電型ソース領域と第二導電型ベース領域との表面に共通に接触して設けられたソース電極と、炭化けい素サブストレートの裏面に設けられたドレイン電極とを有する縦形ＦＥＴにおいて、第二導電型ベース領域の端部の接合深さが第一導電型ソース領域から遠ざかる程ほぼ直線的に浅くなることを特徴とする炭化けい素縦形ＦＥＴ。

【請求項１７】第二導電型ベース領域と一部が重複するように、第二導電型ベース領域より高不純物濃度で、第二導電型ベース領域より接合深さの深い第二導電型コンタクト領域が設けられ、その第二導電型コンタクト領域の表面にソース電極が接することを特徴とする請求項１６記載の炭化けい素縦形ＦＥＴ。

【請求項１８】第二導電型コンタクト領域が埋め込まれて設けられ、第一導電型ソース領域の表面から第二導電型コンタクト領域に達する凹部が設けられて、第二導電型コンタクト領域の露出表面にソース電極が接することを特徴とする請求項１６記載の炭化けい素縦形ＦＥＴ。

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【請求項１９】チャネル領域の不純物濃度が、第一導電型ドリフト層のそれより高濃度であることを特徴とする請求項１６ないし１８のいずれかに記載の炭化けい素縦形ＦＥＴ。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、半導体材料として炭化けい素を用いた、電力用半導体素子である接合型または金属－酸化膜－半導体構造のＭＯＳ型のゲートをもつ縦型電界効果トランジスタ（以下ＦＥＴと記す）の製造方法および縦型電界効果ＦＥＴに関する。

【０００２】

【従来の技術】炭化けい素（以下ＳｉＣと記す）は、バンドギャップが広く、また最大絶縁電界がシリコン（以下Ｓｉと記す）と比較して約一桁大きいことから、次世代の電力用半導体素子への応用が期待されている材料である。これまでに、４Ｈ－ＳｉＣまたは６Ｈ－ＳｉＣと呼ばれる単結晶ウェハを用いて様々な電子デバイスへ応用されつつあり、特に高温、大電力用素子に適すると考えられている。上記の結晶は閃亜鉛鉱型とウルツ鉱型とを積層した形のアルファ相ＳｉＣである。他に３Ｃ－ＳｉＣと称されるベータ相ＳｉＣの結晶でも半導体装置が試作されている。最近では電力用素子としてショットキーダイオード、縦形ＭＯＳＦＥＴ、サイリスタなど、あるいは最も汎用的な半導体装置であるＣＭＯＳ－ＩＣが試作され、その特性から従来のＳｉ半導体装置と比較して非常に特性が良好なことが確認されている［例えば、Weitzel, C. W. 他：IEEE Trans. on Electron Devices, vol. 43, No. 10, pp. 1732-1741 (1997)］。ＭＯＳＦＥＴの幾つかの例を以下に示す。

【０００３】図１３は高周波素子の一つとして開発されている接合型ＦＥＴ（以下ＪＦＥＴと略す）の単位セルの部分断面図である［Sheppard, S. T. 他　, Abstracta of Int. Conf. on Silicon Carbide, III-Nitrides and Related Materials, (1997)］。p^+ 基板１０上に積層されたｎドリフト層１１の表面層にn^+ ソース領域１３、ｐゲート領域１５、n^+ ドレイン領域が形成されている。n^+ ソース領域１３、n^+ ドレイン領域１４、ｐゲート領域１５に接触してそれぞれ、ソース電極１７、ドレイン電極１８、ゲート電極１６が設けられている。

【０００４】この構造では、ゲート電極１６に電圧を印加すると、ｐゲート領域１５からｐゲート領域１５とp^+ 基板１０との間のｎチャネル領域２０に空乏層が広がる。これによってソース電極１７とドレイン電極１８との間の電流が抑制される。また、ゲート電極１６に印加された電圧を取り去ることによって、ドレイン電極１８とソース電極１７との間に再び電流が流れる。このよう

にソース・ドレイン間の電流はゲート電圧によってスイッチング可能な素子となっている。このＪＦＥＴは、ゲート電極１６への電圧印加によってチャネル領域を空乏化するので、デプレッション型と呼ばれる。表面からｐ＋基板１０に達する溝が形成され、絶縁膜１９が充填されているのは、素子分離のためである。

【０００５】一方、図１４は縦型ＭＯＳＦＥＴの１種である[Shenoy, J.N. 他 , Abstracta of Int. Conf. on Silicon Carbide, III-Nitrides and Related Materials, (1997)]。ｎ＋サブストレート２１ａ上に積層されたｎドリフト層２１ｂの表面層に高加速電圧のイオン注入によりｐ＋埋め込み領域２２を形成する。そのｐ＋埋め込み領域２２の上のｎドリフト層部分２１ｂの表面層にｎ＋ソース領域２３が形成されている。二つのｎ＋ソース領域２３に挟まれたｎドリフト層部分２１ｂの表面上にゲート絶縁膜２５を介してゲート電極２６が設けられている。ｎ＋ソース領域２３の表面にソース電極２７が、ｎ＋サブストレート２１ａの裏面にドレイン電極２８がそれぞれ設けられている。

【０００６】この例ではゲート部分がｐｎ接合ではなく、ゲート絶縁膜２５を介して電圧を印加するＭＯＳ構造になっている。このＭＯＳＦＥＴにおいては、ゲート電極層２６に正電圧を印加することによって、ゲート電極２６直下のｎドリフト層２１ｂの表面部分のｎチャネル領域３０に蓄積層が誘起され、ドレイン電極２８と、ソース電極２７との間に電流が流れる。また、ゲート電極２６に負電圧を印加すれば、ドレイン電極２８とソース電極２７との間の電流を遮断することができ、スイッチング機能を有す。ソース・ドレインの間の電圧はｐ＋埋め込み領域２２およびｎドリフト層２１ｂの間に印加されて大きな電圧を保持することが可能であり、高耐圧に適した構造にしたものである。このＭＯＳＦＥＴは、ゲート電極２６への電圧印加によって蓄積層を形成するので、ＡＣＣＵＦＥＴと呼ばれる。

【０００７】図１５は別の縦型高耐圧ＭＯＳＦＥＴのの単位セルの部分断面図である[Onda, S. 他 , Phys. Stat. Sol. (a), vol. 162, p. 369, (1997)]。ｎ＋サブストレート３１ａ上に積層されたｎドリフト層３１ｂの表面層にｐベース領域３２が形成され、そのｐベース領域３２の表面層にｎ＋ソース領域３３が形成されている。二つのｎ＋ソース領域３３をつなぐｎチャネル領域４０がエピタキシャル成長により形成されており、そのｎチャネル領域４０の表面上にゲート絶縁膜３５を介してゲート電極層３６が設けられている。ｎ＋ソース領域３３の表面にソース電極２７が、ｎ＋サブストレート３１ａの裏面にドレイン電極３８がそれぞれ設けられている。

【０００８】この場合も、ゲート電極層３６に正電圧を印加することによって、ゲート電極層３６直下のｎチャネル領域４０の表面部分に蓄積層が誘起され、ドレイン電極３８から、ソース電極３７への電流を流すことが可

能となる。また、ゲート電極層３６に負電圧を印加することによって、ドレイン電極３８とソース電極２７との間が遮断されて、スイッチング機能を示すことになる。

【０００９】他に、プレーナ型、或いはトレンチ型のＭＯＳＦＥＴの試作例もあるが、ＳｉＣでは反転層の移動度が非常に小さいことが実験的にわかっており、反転層を用いるエンハンスメント型のＦＥＴは実用に適さないと考えられる。それに対し、上記三例の素子は反転層を用いるエンハンスメント型のＦＥＴではなく、もともとの導電型の半導体層をチャネルとして用いたＦＥＴであるという点で共通の特徴をもち、特にＳｉＣに適する構造の例である。

【００１０】

【発明が解決しようとする課題】電力用の半導体素子を製造しようとするとき、図１３、１４や図１５の構造は非常に優れた特性が期待されるものの、実際にはこれまであまり良好な特性が実現していないか、または実際には製造されていない。その理由の一つは、Ｓｉ半導体でもっとも普及している方法である二重拡散ＭＯＳ(D-MOS) 構造が、ＳｉＣでは容易に実現できない点にある。Ｓｉでは、ｐ型不純物とｎ型不純物とを同一のマスクにより選択的に導入し、熱拡散することによって、精密なチャネル密度が実現される。すなわちＭＯＳＦＥＴの特性を左右するチャネルの寸法が、非常に精密に制御可能で、歩留まり良くＭＯＳＦＥＴを作ることができる。

【００１１】これにに対し、ＳｉＣではイオン注入した不純物の活性化率が悪く、これを向上させるために、１０００℃以上でのイオン注入、また１６００℃以上での活性化熱処理が必要であり、また、イオン注入した不純物の拡散がほとんど起きない。そのため、ｐ型不純物とｎ型不純物の導入とをそれぞれ別々のマスクによらねばならず、精密なチャネル密度の制御が実現されない。そのため、チャネル抵抗が大きく、またそのバラツキも非常に大きなものとなって、素子全体の抵抗はほぼチャネル抵抗で規定されてしまう程である。ＳｉＣ本来の特性が得られていないといえる。

【００１２】以上の問題に鑑み本発明の目的は、非常に精密なチャネルが実現でき、かつ容易に高耐圧できる炭化けい素縦型ＦＥＴの製造方法および炭化けい素縦型ＦＥＴを提供することにある。

【００１３】

【課題を解決するための手段】上記課題解決のため本発明は、第一導電型炭化けい素サブストレート上に積層された炭化けい素からなる第一導電型ドリフト層と、その第一導電型ドリフト層の表面層に選択的に互いに隔離して形成された第二導電型ゲート領域、第一導電型ソース領域と、その第二導電型ゲート領域および第一導電型ソース領域の下方に選択的に形成された第二導電型埋め込み領域と、第二導電型ゲート領域の表面に接触して設けられたゲート電極層と、第一導電型ソース領域と第二導

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電型埋め込み領域との表面に共通に接触して設けられたソース電極と、炭化けい素サブストレートの裏面に設けられたドレイン電極とを有する縦形ＦＥＴの製造方法において、第一のマスクの一部の一方の端により第一導電型ソース領域の一方の端を規定し、第一のマスクの一部の他方の端と第一のマスクの他の部分とにより第二導電型ゲート領域を規定しと、前記第一のマスクの他の部分により第二導電型埋め込み領域の端を規定するものとする。

【００１４】例えば、具体的な工程としては、第一導電型炭化けい素サブストレート上に炭化けい素からなる第一導電型ドリフト層がエピタキシャル成長により積層された基板を用い、その第一導電型ドリフト層の表面上に第一のマスクを形成する工程と、第一のマスクと一部が重複するように第一のマスクとは異なる材料からなる第二のマスクを形成する工程と、それらのマスクにより選択的に第一導電型ドリフト層の表面層に第一導電型ソース領域形成のための不純物を導入する工程と、第二のマスクを除去する工程と、第一のマスクと一部が重複するように第一のマスクとは異なる材料からなる第三のマスクを形成する工程と、それらのマスクにより選択的に第一導電型ドリフト層の表面層に第二導電型ゲート領域形成のための不純物を導入する工程と、第一のマスクの一部を残して第一のマスク、第三のマスクを除去する工程と、そのマスクにより選択的に第一導電型ドリフト層の表面層に第二導電型埋め込み領域形成のための不純物を導入する工程と、導入した不純物を活性化するための熱処理工程と、炭化けい素基板表面に第四のマスクを形成する工程と、そのマスクにより第一導電型ソース領域の表面から第二導電型埋め込み領域に達する凹部を形成する工程と、絶縁物からなる第五のマスクを形成する工程と、金属膜を蒸着する工程と、その金属膜からなるゲート電極、ソース電極、ドレイン電極を形成する工程とからなるものとする。

【００１５】そのようにすれば、チャネル領域の実質的な寸法は、第二導電型ゲート領域で決まるので、マスク合わせによる不均一が回避され、精密な制御が可能になる。これにより、オン抵抗の小さいＦＥＴを製造することが可能である。第一導電型ソース領域の表面から第二導電型埋め込み領域に達する凹部を形成してソース電極を設ける代わりに、第二導電型埋め込み領域に達する第二導電型コンタクト領域を形成してもよい。そのようにすれば、表面上にソース電極を設けることができる。

【００１６】特に、第一導電型ソース領域、第二導電型ゲート領域、第二導電型埋め込み領域形成のための不純物の導入がいずれもイオン注入によっておこなわれるものとすれば、ＳｉＣにおいても確実に不純物領域の形成ができる。第一導電型ドリフト層の表面とショットキー接合を形成する電極を設けてもよい。

【００１７】そのようにすれば、接触抵抗のために必要

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な第二導電型ゲート領域の寸法より、小さなチャネル領域とすることができる。また、第一導電型炭化けい素サブストレート上に積層された炭化けい素からなる第一導電型ドリフト層と、その第一導電型ドリフト層の表面層に選択的に形成された第一導電型ソース領域と、第一導電型ソース領域の下方に選択的に形成された第二導電型埋め込み領域と、第一導電型ドリフト層の表面上にゲート絶縁膜を介して設けられたゲート電極層と、第一導電型ソース領域と第二導電型埋め込み領域との表面に共通に接触して設けられたソース電極と、炭化けい素サブストレートの裏面に設けられたドレイン電極とを有する縦形ＦＥＴの製造方法において、第一のマスクの一部により第一導電型ソース領域の一方の端を規定し、前記第一のマスクの他の部分により第二導電型埋め込み領域の端を規定するものとする。

【００１８】例えば、具体的な工程としては、第一導電型炭化けい素サブストレート上に炭化けい素からなる第一導電型ドリフト層がエピタキシャル成長により積層された基板を用い、その第一導電型ドリフト層の表面上に第一のマスクを形成する工程と、第一のマスクと一部が重複するように第一のマスクとは異なる材料からなる第二のマスクを形成する工程と、それらのマスクにより選択的に第一導電型ドリフト層の表面層に第一導電型ソース領域形成のための不純物を導入する工程と、第一のマスクの一部を残して第一のマスク、第二のマスクを除去する工程と、それらのマスクにより選択的に第一導電型ドリフト層の表面層に第二導電型埋め込み領域形成のための不純物を導入する工程と、残した第一のマスクの一部を除去する工程と、導入した不純物を活性化するための熱処理工程と、炭化けい素基板表面に熱酸化によりゲート酸化膜を形成する工程と、そのゲート酸化膜上に多結晶シリコン層を堆積した後パターン形成する工程と、絶縁膜を被覆した後第三のマスクを形成する工程と、そのマスクにより第一導電型ソース領域の表面から第二導電型埋め込み領域に達する凹部を形成する工程と、絶縁膜に接触用の窓を設け金属膜を蒸着する工程と、その金属膜からなるゲート電極、ソース電極、ドレイン電極を形成する工程とからなるものとする。

【００１９】この場合も、チャネル領域の寸法は、第一のマスクで決められるので、マスク合わせによる不均一が回避され、精密な制御が可能になる。第一導電型ソース領域の表面から第二導電型埋め込み領域に達する凹部を形成してソース電極を設ける代わりに、第二導電型埋め込み領域に達する第二導電型コンタクト領域を形成してもよい。そのようにすれば、表面上にソース電極を設けることができる。

【００２０】別の方法として、端部がゆるやかなテーパー状の第一のマスクの厚さの厚い部分により第一導電型ソース領域の一方の端を規定し、前記第一のマスクの第一のマスクの厚さの薄い部分により第二導電型ベース領

域の端を規定することもできる。例えば、具体的な工程としては、第一導電型炭化けい素サブストレート上に炭化けい素からなる第一導電型ドリフト層がエピタキシャル成長により積層された基板を用い、その第一導電型ドリフト層の表面上に第一のマスクを形成する工程と、端部がゆるやかなテーパー状の第一のマスクを形成する工程と、そのマスクの厚さの厚い部分により選択的に第一導電型ドリフト層の表面層に第一導電型ソース領域形成のための不純物を導入する工程と、第一のマスクの厚さの厚い部分により選択的に第一導電型ドリフト層の表面層に第二導電型ベース領域形成のための不純物を導入する工程と、炭化けい素基板表面に第三のマスクを形成する工程と、そのマスクにより第二導電型ベース領域に達する第二導電型コンタクト領域形成のための不純物を導入する工程と、第一のマスクを除去する工程と、導入した不純物を活性化するための熱処理工程と、炭化けい素基板表面に熱酸化によりゲート酸化膜を形成する工程と、そのゲート酸化膜上に多結晶シリコン層を堆積した後パターン形成する工程と、絶縁膜を被覆する工程と、絶縁膜に接触用の窓を設け金属膜を蒸着する工程と、その金属膜からなるゲート電極、ソース電極、ドレイン電極を形成する工程とからなるものとする。

【００２１】この場合もチャネル領域の寸法は、第一のマスクで決められるので、マスク合わせによる不均一が回避され、精密な制御が可能になる。しかも、不純物領域形成のための別のマスクを必要としない。第一導電型ソース領域の表面から第二導電型ベース領域に達する凹部を形成し、第一導電型ソース領域と、第二導電型コンタクト領域に接触するソース電極を設けても良い。

【００２２】特に、第一のマスクの側方にサイドウォールを設ける工程と、第一のマスクとサイドウォールをマスクとして、第二導電型コンタクト領域形成のための不純物導入工程が加えられているとよい。そのようにすれば、マスク合わせによらず、第二導電型ベース領域とずらした第二導電型コンタクト領域の形成ができる。

【００２３】第二導電型コンタクト領域形成のための厚さの厚い第三のマスクを形成し、そのマスクにより不純物を導入する工程を先に経た後、その第三のマスクをエッチバックして端部がゆるやかなテーパー状の第一のマスクとすることができる。そのようにすれば、第一のマスクと第三のマスクとはもとは同じものであり、別のマスク材料を形成する必要が無い。

【００２４】更に、第一導電型ソース領域、第二導電型埋め込み領域、第二導電型ベース領域形成のための不純物の導入がいずれもイオン注入によっておこなわれるものとすれば、ＳｉＣにおいても確実に不純物領域の形成ができる。そして、第一導電型ドリフト層の表面層の全面にチャネル領域の不純物濃度制御のための第一導電型不純物を導入する工程が加えられているものとする。

【００２５】チャネル領域の不純物濃度を制御することによって、しきい電圧を制御することができ、また、ノーマリオフのＦＥＴとすることができる。上記のような製造方法により、第一導電型炭化けい素サブストレート上に積層された炭化けい素からなる第一導電型ドリフト層と、その第一導電型ドリフト層の表面層に選択的に少なくとも一部が埋め込まれて形成された第二導電型ベース領域と、その第二導電型ベース領域の上方の一部に第二導電型ベース領域と接して形成された第一導電型ソース領域と、第二導電型ベース領域上に残された第一導電型ドリフト層であるチャネル領域上にゲート絶縁膜を介して設けられたゲート電極層と、第一導電型ソース領域と第二導電型ベース領域との表面に共通に接触して設けられたソース電極と、炭化けい素サブストレートの裏面に設けられたドレイン電極とを有し、第二導電型ベース領域の端部の接合深さが第一導電型ソース領域から遠ざかる程ほぼ直線的に浅くなる炭化けい素縦形ＦＥＴとすれば、チャネル領域の長さの制御が容易であり、均一なチャネル領域を持つ縦形ＦＥＴが容易に製造できる。

【００２６】第二導電型ベース領域と一部が重複するように、第二導電型ベース領域より高不純物濃度で、第二導電型ベース領域より接合深さの深い第二導電型コンタクト領域を設け、その第二導電型コンタクト領域の表面にソース電極を接触させても、第一導電型ソース領域の表面から第二導電型コンタクト領域に達する凹部が設けられて、第二導電型コンタクト領域の露出表面にソース電極を接触させても良い。

【００２７】第一導電型ソース領域と同じ表面で第二導電型コンタクト領域の表面にソース電極を接触させれば、凹部を設ける必要が無く、第一導電型ソース領域の表面から第二導電型コンタクト領域に達する凹部を設けてソース電極を接触させれば、第二導電型コンタクト領域の厚さを厚くする必要が無い。チャネル領域の不純物濃度が、第一導電型ドリフト層のそれより高濃度であるものとすれば、不純物濃度を制御することによって、しきい電圧を制御することができ、また、ノーマリオフのＦＥＴとすることができる。

【００２８】

【発明の実施の形態】以下本発明について、実施例を示しながら詳細に説明する。ただし、図１３～１５と共通の部分、あるいは本発明とかかわりのない部分については説明を省略する。本発明の重要な応用例としてｎチャネルＭＯＳＦＥＴを例に取っているが、導電型を逆にしたｐチャネルＭＯＳＦＥＴにも本発明が適応可能なことは勿論である。なお、ここで説明する炭化けい素は良く知られているように、多くのポリタイプが存在するが、主に６Ｈおよび４Ｈと呼ばれるものを対象としている。

【００２９】［実施例１］図１は本発明第一の実施例（以下実施例１と記す。以下同様）にかかるＳｉＣＪＦＥＴの単位セルの断面図である。これは図１３の従来素子を高耐圧化した素子に対応している。n^+ サブストレ

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ート４１ａ上にエピタキシャル成長によりｎドリフト層４１ｂが積層されたウェハにおいて、ｎドリフト層４１ｂの表面から少し深い位置にｐ⁺ 埋め込み領域４２が形成され、ｐ⁺ 埋め込み領域４２の上方のｎドリフト層４１ｂの表面層にはｐゲート領域４４とｎ⁺ ソース領域４３とが形成されている。ｐゲート領域４４の表面上にはゲート電極４６が設けられている。ｎ⁺ ソース領域４３の表面から掘り下げられた凹部４７ａの表面に沿って、ｎ⁺ ソース領域４３とｐ⁺ 埋め込み領域４２との表面に共通に接触してソース電極４７が設けられ、またｎ⁺ サブストレート４１ａの裏面に接触してドレイン電極４８が設けられている。

【００３０】主なディメンジョンの一例は、次のような値である。ｎ⁺ サブストレート４１ａの不純物濃度は１×１０^{18}ｃｍ^{3} 、厚さ３５０μｍ、ｎドリフト層４１ｂのそれは、１×１０^{16}ｃｍ^{3} 、厚さ１０μｍ。ｐ⁺ 埋め込み領域４２の最高不純物濃度は５×１０^{18}ｃｍ^{3} 、厚さ０．５μｍで、その上に０．５μｍのｎドリフト層４１ｂがある。両側のｐ⁺ 埋め込み領域４２の間の間隔は、約５μｍである。ｎ⁺ ソース領域４３の不純物濃度は１×１０^{19}ｃｍ^{3} 、接合深さ０．２μｍで、幅は約３μｍ、ｐゲート領域４４のそれは、５×１０^{18}ｃｍ^{3} 、接合深さ０．２μｍ、幅は約２μｍである。ｎ⁺ ソース領域４３とｐゲート領域４４との間の間隔は約１μｍであり、ｎドリフト層４１ｂが表面に達している。表面から掘り下げられた凹部４７ａの深さは、０．７μｍで、幅は約３μｍである。図の単位セルのピッチは約２５μｍである。

【００３１】図１３の横型ＪＦＥＴと違っている点は、ソース電極４７とドレイン電極４８とが半導体基板の両面に設けられた縦型のＦＥＴとなっている点であるが、その動作は、基本的には図１１のものと変わらない。すなわち、ゲート電極４６に電圧を印加することによって、ｐゲート領域４４から下方のチャネル領域５０に空乏層が広がり、ｎ⁺ ソース領域４３とｎドリフト層４１ｂとが電気的に絶縁される。その結果ドレイン電極３８からソース電極３７への電流が抑制される。図１３に示したものと同じデプレッションタイプのＪＦＥＴである。

【００３２】図２（ａ）ないし（ｆ）および図３（ａ）ないし（ｄ）は、図１の実施例１のＳｉＣＪＦＥＴの製造方法を説明するための製造工程順の表面近傍の部分断面図である。以下順に説明する。先ず、ｎ⁺ サブストレート４１ａ上に燐ドープのｎドリフト層４１ｂをエピタキシャル成長により積層した４Ｈ－ＳｉＣ基板を準備する。例えば、ｎドリフト層４１ｂの不純物濃度は１×１０^{16}ｃｍ$^{-3}$、厚さは１０μｍである。そのｎドリフト層４１ｂの表面上に、多結晶シリコン膜１を減圧ＣＶＤ法により堆積し、フォトリソグラフィでパターンを形成して、第一マスクＭ１とする［図２（ａ）］。第一マスク

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Ｍ１は、中央部のＭ１ａと両側のＭ１ｂの各部分からなる。多結晶シリコン膜１の厚さは１μｍとした。第一マスクＭ１は必ずしも多結晶シリコン膜である必要はなく、選択的なエッチングのマスクとなるものであれば、シリコンプロセスなどによく用いられる酸化けい素膜（以下ＳｉＯ$_2$ 膜と記す）、窒化けい素膜あるいはフォトレジストであってもよい。但し高温でイオン注入をする場合には、多結晶シリコンなどの高温に絶える材料を用いる必要がある。

【００３３】多結晶シリコン膜１の第一マスクＭ１の上に熱ＣＶＤ法によりＳｉＯ$_2$ 膜２を堆積し、フォトリソグラフィでパターンを形成して、第二マスクＭ２とした後、これら第一、第二マスクＭ１、Ｍ２により規定された領域に、ｎ型不純物となるイオン例えば窒素（以下Ｎと記す）イオン４ａを注入する［同図（ｂ）］。４ｂは注入されたＮ原子である。これはｎ⁺ ソース領域４３形成のためであり、加速電圧は１００ｋｅＶ、ドーズ量は約５×１０^{15}ｃｍ$^{-2}$である。イオン注入時の温度は、約８００℃である。高温でイオン注入することにより、活性化率を向上させることができる。第二マスクＭ２は、必ずしもＳｉＯ$_2$ 膜である必要はないが、後の工程で第一マスクＭ１を残したまま除去することが必要であるため、第一マスクＭ１とは異なる材料とし、選択的なエッチングができるようにする必要がある。例えば、第一マスクＭ１として多結晶シリコン膜を使用した場合、第二マスクＭ２として、上の例のようにＳｉＯ$_2$ 膜を用いれば、ふっ酸により第二マスク２だけを除去可能である。その逆も可能であり、その場合には四塩化炭素と酸素の混合ガス等を用いた反応性イオンエッチング（以下ＲＩＥと記す）により、ＳｉＯ$_2$ 膜と多結晶シリコン膜のエッチング速度を制御して多結晶シリコン膜のみをエッチングすることが可能である。このように、第一マスクＭ１に対して選択的な除去のできるものであればよい。第二のマスクＭ２は、端が第一マスクＭ１上にあれば良いのでマスク合わせは容易である。ｎ型不純物としてはＮの他に燐（以下Ｐと記す）などが用いられる。

【００３４】ＳｉＯ$_2$ 膜の第二マスクＭ２を除去し、再度熱ＣＶＤ法によりＳｉＯ$_2$ 膜２を堆積し、フォトリソグラフィでパターンを形成して、第三マスクＭ３とした後、これら第一、第三マスクＭ１、Ｍ３で規定される領域に、ｐ型不純物となるイオン例えばほう素（以下Ｂと記す）イオン５ａを注入する［同図（ｃ）］。５ｂは注入されたＢ原子である。これはｐゲート領域４４形成のためであり、加速電圧は１００ｋｅＶ、ドーズ量は約５×１０^{15}ｃｍ$^{-2}$である。この場合も第三マスクＭ３は必ずしもＳｉＯ$_2$ 膜である必要はなく、後の工程で第一マスクＭ１に対して選択的な除去のできるものであればよい。第三マスクＭ３は、端が第一のマスクＭ１上にあれば良いのでマスク合わせは容易である。ｐ型不純物となる不純物としてはＢの他にアルミニウム（以下Ａｌと記

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す）などを用いることができる。

【００３５】SiO_2 膜の第三マスクＭ３を除去し、フォトリソグラフィでと第一マスクの一部Ｍ１ｂも除去し、第一マスクの一部Ｍ１ａを残す［同図（ｄ）］。残した第一マスクの一部Ｍ１ａをマスクにして再びＢイオン５ａを注入する。［同図（ｅ）］。これはp^+ 埋め込み領域４２形成のためであり、加速電圧は４００ｋｅＶ、ドーズ量は約$1\times10^{15}cm^{-2}$である。加速電圧を高めたのは、深い不純物領域を形成するためである。ｐ型不純物としてはＢの他にＡｌなどを用いてもよい。

【００３６】残した第一マスクの一部Ｍ１ａを除去し、全面にＮイオン４ａを注入する。［同図（ｆ）］。４ｂは注入されたＮ原子である。これはｎチャネル領域５０の濃度制御のためであり、加速電圧は２００ｋｅＶ、ドーズ量は約$1\times10^{12}cm^{-2}$である。この前にp^+ 埋め込み領域４２のための深いイオン注入をおこなっているため、p^+ 埋め込み領域４２の上になる表面層のｎドリフト層４１ｂにはＢ原子が注入されている。Ｎイオンの注入により、表面層の抵抗を安定させることができる。熱処理後の表面層の不純物濃度は、約$5\times10^{15}cm^{-3}$になる。

【００３７】１６００℃、２時間の熱処理をおこない、注入した不純物を活性化することによってn^+ ソース領域４３、ｐゲート領域４４、p^+ 埋め込み領域４２の各領域が形成される［図３（ａ）］。先に述べたようにＳｉＣでは不純物の拡散が殆ど起きないが、加速電圧の調節により、不純物領域の形成される深さを制御することができる。例えば、p^+ 埋め込み領域４２は、加速電圧を４００ｋｅＶと高くしたことによって、深さ０．８μｍを中心にして、厚さ０．５μｍの層ができており、その上には約０．５μｍのｎドリフト領域４１ｂが残されている。ｐゲート領域４４、n^+ ソース領域４３の深さは、約０．２μｍである。

【００３８】表面に、ＣＶＤ法により、SiO_2 膜２を堆積する［同図（ｂ）］。フォトリソグラフィで第四マスクＭ４を形成し、四フッ化炭素（CF_4）と酸素（O_2）との混合ガスを用いたＲＩＥで、n^+ ソース領域４３の表面からp^+埋め込み領域４２に達する凹部４７ａを形成する［同図（ｃ）］。フォトリソグラフィでSiO_2 膜２にコンタクト用の開口を形成した後、アルミニウム合金膜を蒸着し、パターン形成して、ソース電極４７およびゲート電極４６とする。n^+ サブストレートの裏面にもドレイン電極を設けてプロセスを完了する［同図（ｄ）］。

【００３９】上記のような製造方法をとることにより、図１の高耐圧ＳｉＣ縦型ＪＦＥＴとすることができた。実施例１のＳｉＣＪＦＥＴでは、第一マスクの一部Ｍ１ｂの端によってn^+ ソース領域４３が規定され、第一マスクの一部Ｍ１ｂの別の端と、第一マスクの別の部分Ｍ１ａとによってｐゲート領域４４が規定されている。さ

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らに第一マスクの別の部分Ｍ１ａによって、p^+ 埋め込み領域４２の端が規定されている。このように、不純物領域が第一マスクＭ１だけで規定されているため、それぞれが整合しており、位置ずれ等のマスク合わせによる不均一の問題が起こり得ない。第一マスクＭ１のパターン形成後に、各不純物領域の寸法が確認できるという利点もある。

【００４０】チャネル領域の長さはＭＯＳＦＥＴの特性を決定する主たるパラメータであることから、その制御は応用上極めて重要であるが、本実施例１のＳｉＣＪＦＥＴでは、実質的にチャネル長となるのは、ｐゲート領域４４の下部のｎチャネル領域５０であり、チャネル長が短く均一に、精度よく形成され、安定した特性と高い歩留まりが得られる。試作した１５００ＶクラスのＪＦＥＴのオン抵抗は、$15m\Omega\cdot cm^{-2}$と低い値を示した。

【００４１】また、p^+ 埋め込み領域４２を加速電圧の高いイオン注入で形成して、接合深さを深くしたため、容易に１５００Ｖ以上の高耐圧が実現できた。ｎドリフト層４１ｂの表面層に不純物濃度制御のためのＮイオン注入工程が加えられたことによって、ＭＯＳＦＥＴのしきい電圧を制御することができ、ノーマリオフのＦＥＴとすることもできる。

【００４２】製造方法としては、幾つかの変形も考えられる。例えば、n^+ ソース領域４３とｐゲート領域４４とを形成するためのイオン注入の順序は逆でもよい。また、ｎチャネル領域５０の不純物濃度制御のためのイオン注入は最初におこなってもよい。イオン注入を１０００℃というような高温でなく、もっと低温でおこなうことにすれば、マスク材料の選択幅が広げられる。

【００４３】［実施例２］図４は本発明第二の実施例にかかるＳｉＣＪＦＥＴの部分断面図である。これは図１の実施例１の変形例である。この例では、ＳｉＣ基板表面に凹部が形成されず、ｎドリフト層５１ｂの表面層にp^+ 埋め込み領域５２に達するp^+ コンタクト領域５２ａが形成されていて、その表面にn^+ ソース領域５３と共通のソース電極５７が設けられている。

【００４４】n^+ ソース領域５３形成のためのＮイオン注入の際の（図２（ｂ）のＭ２に相当する）マスクとして、n^+ ソース領域５３の外側をも規定するマスクを使用し、更に別のマスクを用いてp^+ コンタクト領域５２ａ形成のためのＢイオン注入を行えば良い。このようにすれば、凹部を形成せず、基板表面に電極を設けることができる。

【００４５】n^+ ソース領域５３の内側を規定するのは、第一マスクの一部（図２（ｂ）のＭ１ｂに相当する）であることに代わりは無く、チャネル領域の長さは実施例１のＳｉＣＪＦＥＴと同様であり、ｐゲート領域４４の下部のｎチャネル領域６０は、チャネル長が短く均一で、精度よく形成され、安定した特性と高い歩留ま

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りが得られる。

【００４６】［実施例３］図５は本発明第三の実施例にかかるＳｉＣＪＦＥＴの部分断面図である。これも図１のＳｉＣＪＦＥＴの変形ともいえる。図１のＳｉＣＪＦＥＴと違っている点は、ゲート電極６６がｐゲート領域６４とｎドリフト層６１ｂの表面に共通に接触している点である。ここで、ゲート電極６６は、ＳｉＣ基板とショットキー接合を形成するような金属、例えばＴｉ，Ａｌ、Ｐｔなどを選択する。

【００４７】実施例１のＪＦＥＴでは図１からわかるように、ｐゲート領域４４はゲート電極４６が接触する部分でのみコンタクトが取られている。この接触抵抗を小さく抑えるためには、接触面積を大きくしなければならず、このコンタクト窓の大きさがチャネルの長さの最低値を制限していた。本実施例３のＪＦＥＴはこの点を改良したものであり、ゲート電極６６がｐゲート領域６４だけでなく、ｎドリフト層６１ｂの表面にも接触しているため、コンタクト部分が広く取れ、チャネル領域を狭く設計することが可能となる。

【００４８】この実施例３のＪＦＥＴにおいても、n^+ ソース領域がｐベース領域の表面層に自己整合して形成されており、実施例１のＪＦＥＴと同様にチャネル長が、均一で精度よく形成され、安定した特性が歩留まりよく得られることは同じである。ただし、ゲート電極６６は、ＳｉＣ基板とショットキー接合を形成するような金属であり、ソース電極６７と同じ金属とは限らない。或いは、ゲート電極６６は、ショットキー接触をする金属とソース電極６７と同じ金属との二層にしてもよい。これを製造するプロセスについてはほとんど図２、３とほぼ同一であり、説明を省く。

【００４９】［実施例４］図６は本発明第四の実施例にかかるＳｉＣＭＯＳＦＥＴの部分断面図である。n^+ サブストレート７１ａ上にエピタキシャル成長によりｎドリフト層７１ｂが積層されたウェハにおいて、ｎドリフト層７１ｂの表面から少し深い位置に p^+ 埋め込み領域７２が形成され、その p^+ 埋め込み領域７２の上方のｎドリフト層７１ｂの表面層に n^+ ソース領域７３が形成されている点は、これまでの例と同じであるが、ｐゲート領域はなく、p^+ 埋め込み領域７２の上方は、ｎチャネル領域８０とされ、その表面上にＭＯＳ構造のゲートが設けられている。

【００５０】すなわち、ｎドリフト層７１ｂの表面上に、ゲート酸化膜７５を介して多結晶シリコン層からなるゲート電極層７６が設けられている。７９はゲート電極層７６と、ソース電極７７とを絶縁するほう素燐シリカガラス（ＢＰＳＧ）の絶縁膜である。n^+ ソース領域７３の表面から掘り下げられた凹部７７ａがあり、その表面に沿って、n^+ ソース領域７３と p^+ 埋め込み領域７２との表面に共通に接触するソース電極７７が設けられ、また n^+ サブストレート７１ａの裏面に接触してドレイン電極７８が設けられている。主な各部のディメンジョンは、実施例１で述べた値とほぼ同じである。ゲート酸化膜７５の厚さは５０ｎｍ、ゲート電極層７６の厚さは１μｍ、絶縁膜７９の厚さは２μｍである。

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【００５１】このＭＯＳＦＥＴもＡＣＣＵＦＥＴと呼ばれるものであり、ゲート電極層７６に正電圧を印加することによって、ゲート電極層７６直下のｎドリフト層７１ｂの表面部分に蓄積層が誘起され、ドレイン電極７８と、ソース電極７７との間に電流が流れる。また、ゲート電極層７６に負電圧を印加すれば、ドレイン電極７８とソース電極７７との間の電流を遮断することができ、スイッチング機能を有す。ソース・ドレインの間の電圧は p^+ 埋め込み領域７２およびｎドリフト層７１ｂの間に印加されて大きな電圧を保持することが可能であり、高耐圧に適した構造になっている。

【００５２】図７（ａ）ないし（ｅ）および図８（ａ）ないし（ｄ）は、図６の実施例４のＳｉＣＭＯＳＦＥＴの表面近傍の製造工程順の部分断面図である。以下順に工程について説明する。n^+ サブストレート７１ａ上に燐ドープのｎドリフト層７１ｂをエピタキシャル成長により積層した４Ｈ－ＳｉＣ基板を準備する。ｎドリフト層７１ｂの不純物濃度、厚さ等は実施例１と同じでよい。そのｎドリフト層７１ｂの表面上に、多結晶シリコン膜を減圧ＣＶＤ法により堆積し、フォトリソグラフィでパターンを形成して、第一マスクＭ１とする［図７（ａ）］。第一マスクＭ１は、中央部のＭ１ａと両側のＭ１ｂの各部分からなる。第一マスクＭ１は必ずしも多結晶シリコン膜である必要がないのは実施例１と同じである。

【００５３】多結晶シリコン膜の第一マスクＭ１の上に熱ＣＶＤ法により SiO_2 膜を堆積し、フォトリソグラフィでパターンを形成して、第二マスクＭ２とした後、これら第一、第二マスクＭ１、Ｍ２により規定された領域に、ｎ型不純物となるイオン例えばＮイオン４ａを注入する［同図（ｂ）］。これは n^+ ソース領域７３形成のためであり、加速電圧、ドーズ量等は実施例１と同じでよい。この第二マスクＭ２は、必ずしも SiO_2 である必要はないが、後の工程で第一マスクＭ１を残したまま除去することが必要であるため、第一マスクＭ１とは異なり、選択的なエッチングができる材料を選ぶ。第二マスクＭ２は、端が第一マスクＭ１上にあれば良いのでマスク合わせは容易である。ｎ型不純物としてはＮの他にＰなどが用いられる。

【００５４】SiO_2 膜の第二マスクＭ２を除去し、フォトリソグラフィで第一マスクの一部Ｍ１ａを残した後、ｐ型不純物となるイオン例えばＢイオン５ａを注入する［同図（ｃ）］。これは p^+ 埋め込み領域７２形成のためであり、加速電圧は４００ｋｅＶ、ドーズ量は約 $1\times10^{15}\,cm^{-2}$ である。加速電圧を高めたのは、深い不純物領域を形成するためである。ｐ型不純物はＢの他

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にＡｌなどが用いられる。

【００５５】残した第一マスクの一部Ｍ１ａを除去し、Ｎイオン４ａを注入する。［同図（ｄ）］。これはｎチャネル領域８０の不純物濃度制御のためであり、加速電圧は２００ｋｅＶ、ドーズ量は約$1\times10^{12}cm^{-2}$である。１６００℃、２時間の熱処理をおこない、注入した不純物を活性化することによって、p^+埋め込み領域７２、n^+ソース領域７３、ｎチャネル領域８０の各領域が形成される［同図（ｅ）］。

【００５６】表面に、１２００℃、２時間の熱酸化によりゲート酸化膜７５となるSiO_2膜を形成し、続いて減圧ＣＶＤ法によりゲート電極層となる多結晶シリコン膜１を約１μｍ堆積する［図８（ａ）］。ゲート酸化膜７５は熱酸化で形成する他に、ＣＶＤにより成膜することも可能である。ゲート電極層７６の材料としては多結晶シリコンの他にモリブデン（Ｍｏ）などが使用可能である。

【００５７】フォトレジストを塗布し、フォトリソグラフィで多結晶シリコン膜１をパターン形成してゲート電極層７６とした後、表面にＣＶＤ法により、ほう素燐シリカガラス（ＢＰＳＧ）などの絶縁膜７９を堆積する［同図（ｂ）］。フォトリソグラフィでパターンを形成し、四フッ化炭素（CF_4）と酸素（O_2）との混合ガスを用いたＲＩＥで、n^+ソース領域７３の表面からp^+埋め込み領域７２に達する凹部７７ａを形成する［同図（ｃ）］。

【００５８】フォトリソグラフィで絶縁膜７９にコンタクト用の開口を形成した後、アルミニウム合金を蒸着し、パターン形成して、ソース電極７７および図示しないゲート電極とする。n^+サブストレートの裏面にもドレイン電極を設けてプロセスを完了する［同図（ｄ）］。この実施例４のＭＯＳＦＥＴにおいても、第一マスクの一部Ｍ１ｂの端によってn^+ソース領域７３が規定され、第一マスクの別の部分Ｍ１ａによって、p^+埋め込み領域７２の端が規定されている。このように、不純物領域が第一マスクＭ１だけで規定されているため、それぞれが整合しており、位置ずれ等のマスク合わせによる不均一の問題が起こり得ない。

【００５９】従って、実施例１のＪＦＥＴと同様に１．５μｍ程度のチャネル長が、均一で精度よく実現され、安定した特性が歩留まりよく得られる。第一マスク１の形成後に、各不純物領域の寸法が確認できるという利点もある。ｎドリフト層７１ｂの表面層に不純物濃度制御のためのＮイオン注入工程が加えられてｎチャネル領域８０とされていることによって、ＭＯＳＦＥＴのしきい電圧を制御することができ、特に、ノーマリオフのＦＥＴとすることもできる。

【００６０】また、ゲート酸化膜７５がＳｉＣ基板上に平面状に形成されているので、従来のトレンチタイプのＭＯＳＦＥＴで見られたゲート酸化膜のコーナー部における電界のストレスの問題が無く、高耐圧化が可能である。製造方法としては、幾つかの変形も考えられる。例えば、ｎチャネル領域８０の不純物濃度制御のためのイオン注入は最初におこなってもよいし、第二マスクＭ２と第三マスクＭ３との形成は逆の順でも良い。

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【００６１】n^+ソース領域７３形成のためのＮイオン注入の際に、n^+ソース領域７３の外側を規定するマスクを使用し、更に別のマスクを用いてp^+コンタクト領域５２ａ形成のためのＢイオン注入を行えば、凹部７７ａを形成せず、基板表面に電極を設けることができる。その場合も　チャネル領域の長さは実施例４のＳｉＣＭＯＳＦＥＴと同様に、均一に、精度よく形成され、安定した特性と高い歩留まりが得られる。

【００６２】［実施例５］図９は本発明第五の実施例にかかるＳｉＣＭＯＳＦＥＴの部分断面図である。n^+サブストレート８１ａ上にエピタキシャル成長により堆積したｎドリフト層８１ｂの表面から少し深い位置にp^+埋め込み領域８２が形成され、p^+埋め込み領域８２の上方のｎドリフト層８１ｂの表面層にｐベース領域８２が形成され、その上方には選択的にn^+ソース領域８３が形成されている。そしてｐベース領域８２の端の部分は、n^+ソース領域８３から遠ざかる程、ほぼ直線的に接合深さが浅くなっているのが特徴的である。また、ｐベース領域８２と一部重複するように、ｐベース領域８２より深い部分にp^+コンタクト領域８２ａが形成されている。n^+ソース領域８３が形成されていない部分のｐベース領域８２の上方は、ｎチャネル領域９０とされ、その上には図６のＭＯＳＦＥＴと同様のＭＯＳ構造のゲートが設けられている。すなわち、ゲート酸化膜８５を介して多結晶シリコン層からなるゲート電極層８６が設けられている。８９はゲート電極層と、ソース電極８７とを絶縁するＢＰＳＧの絶縁膜である。n^+ソース領域８３の表面から掘り下げられた凹部８７ａがあり、n^+ソース領域８３とp^+コンタクト領域８２との表面に共通に接触してソース電極８７が設けられ、またn^+サブストレート８１ａの裏面に接触してドレイン電極８８が設けられている。

【００６３】主なディメンジョンの一例は、次のような値である。n^+サブストレート４１ａの不純物濃度は$1\times10^{18}cm^3$、厚さ３５０μｍ、ｎドリフト層４１ｂのそれは、$1\times10^{16}cm^3$、厚さ１０μｍ。ｐベース領域８２の最高不純物濃度は$5\times10^{16}cm^3$、接合深さ１．５μｍ、両側のｐベース領域８２の間の間隔は、約６μｍである。n^+ソース領域４３の不純物濃度は$1\times10^{19}cm^3$、接合深さ０．２μｍで、幅は約５μｍ、p^+コンタクト領域８２の最高不純物濃度は$1\times10^{19}cm^3$、接合深さ２．０μｍ、幅は約５μｍ、ｎチャネル領域９０の不純物濃度は$5\times10^{15}cm^3$、接合深さ０．５μｍである。n^+ソース領域８３の端とｐベース領域８２の端との間の間隔は約２μｍである。表面

から掘り下げられた凹部８７ａの深さは、０．７μｍで、幅は約３μｍである。図の単位セルのピッチは約３０μｍである。ゲート酸化膜８５の厚さは５０ｎｍ、ゲート電極層８６の厚さは１μｍ、絶縁膜８９の厚さは２μｍである。

【００６４】図１０（ａ）ないし（ｅ）および図１１（ａ）ないし（ｅ）は、図９の実施例５のＳｉＣＭＯＳＦＥＴの表面近傍の製造工程順の部分断面図である。以下順に工程について説明する。先ず、n^+ サブストレート上に燐ドープのｎドリフト層８１ｂをエピタキシャル成長により積層した４Ｈ－ＳｉＣ基板を準備する。ｎドリフト層８１ｂの表面上に、多結晶シリコン膜を減圧ＣＶＤ法により堆積し、フォトリソグラフィでパターンを形成して、第一マスクＭ１とする。

【００６５】特にこのパターニングの際、第一マスクＭ１の端部に１～２μｍにわたりテーパー部８を形成することが重要である。これは、次のｐベース領域形成のためのイオン注入においてチャネル長が第一マスクＭ１のテーパ部８の角度で制御されるからである。従って、このテーパー角度は所定の設計に乗っ取って決められなければならない。そしてこの角度は、第一マスク１の薄膜をプラズマエッチング等によりエッチングする際のエッチング条件を選ぶことによって制御可能である。或いは、薄膜の上部にイオン注入するなどしてダメージを与えておき、表面近傍のみをエッチングされやすくしておくと、ゆるやかなテーパが得られる。その際のイオン注入のドーズ量を制御することにより、テーパ角を制御する方法もある。

【００６６】その第一マスクＭ１をマスクとしてｐ型不純物となるイオン例えばほう素（Ｂ）イオン５ａを注入する［図１０（ａ）］。５ｂは注入されたＢ原子である。これはｐベース領域８２形成のためであり、加速電圧は３００ｋｅＶ、ドーズ量は約1×10^{15} cm^{-2}である。加速電圧を高めたのは、深い不純物領域を形成するためである。第一マスクＭ１の無い領域では不純物は深く注入され、第一マスクＭ１が厚さが増すに従ってほぼ直線的に次第に浅くなって、不純物原子は図のような分布をする。第一マスクＭ１の厚さをある程度薄くしておけば、不純物注入領域は表面にまで達せず、埋め込み型の領域とすることができる。ｐ型不純物はＢの他にＡｌなどが用いられる。第一マスクＭ１は必ずしも多結晶シリコン膜である必要はないのは実施例１と同じである。

【００６７】次に同じ第一マスクＭ１をマスクとしてｎ型不純物となるイオン例えばＮイオン４ａを注入する［同図（ｂ）］。４ｂは注入されたｎ原子である。これはn^+ソース領域８３形成のためであり、加速電圧等は実施例１と同じ１００ｋｅＶ、ドーズ量は約5×10^{15} cm^{-2}でよい。この場合も、第一マスクＭ１の無い領域では不純物は深く注入され、第一マスクＭ１が厚くなると次第に浅くなって、不純物原子は図のような分布をする。但し、加速電圧を低くしているので、注入される領域がＢイオンの注入領域と異なる。テーパー部８の角度が同じであれば、ｐ型不純物の注入領域とｎ型不純物の注入領域との間隔は一定になる。

【００６８】多結晶シリコン膜の第一マスクＭ１の上に熱ＣＶＤ法によりSiO_2 膜２を堆積する［同図（ｃ）］。ＲＩＥで全面エッチングすることにり、第一マスクＭ１のテーパ部８の側方にサイドウオール９を形成した後、これら第一マスクＭ１およびサイドウオール９により規定された領域に、ｐ型不純物となるイオン例えばＢイオン５ａを注入する［同図（ｄ）］。これは高濃度のp^+ コンタクト領域８４形成のためであり、加速電圧、４００ｋｅＶ、ドーズ量は約1×10^{15} cm^{-2}である。ｐ型不純物としてはＢの他にＡｌなどが用いられる。

【００６９】第一マスクＭ１、サイドウォール９を除去した後、全面にＮイオン４ａを注入をする。［同図（ｅ）］。これはｎチャネル領域９０の不純物濃度制御のためであり、加速電圧は２００ｋｅＶ、ドーズ量は約1×10^{12} cm^{-2}である。これにより、例えばしきい値が制御できる。１６００℃、２時間の熱処理をおこない、注入した不純物を活性化することによって各領域が形成される［図１１（ａ）］。このようにして、ｐベース領域８２ sn^+ ソース領域８３とをずらして形成することができる。

【００７０】表面に、１２００℃、２時間の熱酸化によりゲート酸化膜８５となる厚さ５０ｎｍの熱SiO_2 膜６を形成し、続いて減圧ＣＶＤ法により多結晶シリコン膜１を約１μｍ堆積する［同図（ｂ）］。ゲート酸化膜８５は熱酸化で形成する他に、ＣＶＤにより成膜することも可能である。フォトレジストを塗布し、フォトリソグラフィで多結晶シリコン膜１をパターン形成してゲート電極層８６とした後、表面にＣＶＤ法により、ほう素燐シリカガラス（ＢＰＳＧ）などの絶縁膜８９を堆積し、フォトリソグラフィでパターンを形成する［同図（ｃ）］。

【００７１】四フッ化炭素（CF_4）と酸素（O_2）との混合ガスを用いたＲＩＥで、n^+ソース領域８３の表面からp^+ コンタクト領域８２ａに達する凹部８７ａを形成する［同図（ｄ）］。フォトリソグラフィで絶縁膜８９にコンタクト用の開口を形成した後、アルミニウム合金を蒸着し、パターン形成して、ソース電極８７および図示しないゲート電極とする［同図（ｅ）］。n^+ サブストレートの裏面にもドレイン電極を設けてプロセスを完了する。

【００７２】この実施例５のＭＯＳＦＥＴにおいては、第一マスク１の端部をテーパー状とし、ｐ型不純物とｎ型不純物の注入の際の加速電圧を変えることによって、n^+ソース領域８３とｐベース領域８２の端が規定されている。すなわち両者の間の間隔であるチャネル長は第

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一マスクＭ１のテーパー部８で規定される。このように、不純物領域が第一マスクだけで規定されているため、両者が整合しており、位置ずれ等のマスク合わせによる不均一の問題が起きない。

【００７３】従って、チャネル長が均一に精度よく形成され、安定した特性が歩留まりよく得られる。また、第一マスクＭ１のテーパー部８の角度を変えれば、両者の間隔すなわちチャネル領域の長さは自由に制御できることになり、オン抵抗と耐圧のバランスも取りやすい。第一マスク１の形成後に、各不純物領域の寸法が確認できるという利点もある。

【００７４】ｎドリフト層８１ｂの表面層に不純物濃度制御のためのＮイオン注入工程が加えられたことによって、ＭＯＳＦＥＴのしきい電圧を制御することができ、特に、ノーマリオフのＦＥＴとすることもできる。製造方法としては、幾つかの変形も考えられる。例えば、ｎチャネル領域９０の不純物濃度制御のためのイオン注入は最初におこなってもよい。また、ｐベース領域８２のためのＢイオンの注入とｎ$^+$ ソース領域８３形成のためのＮイオンの注入の順は逆でもよい。最初にサイドウォール領域を形成し、ｐ$^+$ コンタクト領域８４形成のためのイオン注入をおこなっても良い。

【００７５】この例でもゲート酸化膜８５がＳｉＣ基板上に平面状に形成されているので、従来のトレンチタイプのＭＯＳＦＥＴで見られたゲート酸化膜コーナー部における電界のストレスの問題が無く、高耐圧化が可能である。また、この実施例では、ｐ$^+$ コンタクト領域８２ａを埋め込み型の領域としたが、ｎ$^+$ ソース領域８３形成のためのＮイオン注入の際に、ｎ$^+$ ソース領域８３の外側を規定するマスクを使用し、ｐ$^+$ コンタクト領域８２ａを多重注入により表面にまで達するようにすれば、基板表面にソース電極８７を設けることができて、凹部８７ａを形成する必要が無い。

【００７６】［実施例６］図１２（ａ）ないし（ｅ）は、図９のＳｉＣＭＯＳＦＥＴとほぼ同じＳｉＣＭＯＳＦＥＴの別の製造方法を説明するための製造工程順の表面近傍の部分断面図である。以下順に工程について説明する。先ず、ｎ$^+$ サブストレート上に燐ドープのｎドリフト層９１ｂをエピタキシャル成長により積層した４Ｈ－ＳｉＣ基板を準備する。ｎドリフト層９１ｂの不純物濃度、厚さ等は実施例１と同じでよい。そのｎドリフト層９１ｂの表面上に、プラズマＣＶＤ法により厚さ約２μｍのSiO_2 膜２を堆積し、フォトリソグラフィでパターンを形成して、第三マスクＭ３とする。

【００７７】その第三マスクＭ３をマスクとしてｐ型不純物となるイオン例えばＢイオン５ａを注入する［図１２（ａ）］。５ｂは注入されたＢ原子である。これは高濃度のｐ$^+$ コンタクト領域９４形成のためであり、加速電圧、４００ｋｅＶ、ドーズ量は約$1\times10^{15}cm^{-2}$である。ｐ型不純物としてはＢの他にＡｌなどが用いられる。

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【００７８】次に、CF_4+H_2 ガスを用いたプラズマエッチングにより、第三マスクＭ３をエッチバックして、端を１～２μｍにわたりテーパー状にした第一マスクＭ１とする［同図（ｂ）］。このとき、全体の厚さも薄くなり、厚さは約１μｍになる。これは、実施例５のＳｉＣＭＯＳＦＥＴの時と同様に、次のｐベース領域形成のためのイオン注入においてチャネルが第一マスクの端部のテーパ角度で制御されるようにするものである。

【００７９】その端部をテーパー状にした第一マスクＭ１をマスクとしてｐ型不純物となるイオン例えばＢイオン５ａを注入する［同図（ｃ）］。これはｐベース領域９２形成のためであり、加速電圧は３００ｋｅＶ、ドーズ量は約$1\times10^{15}cm^{-2}$である。第一マスクＭ１の無い領域では不純物は深く注入され、第一マスクＭ１が厚さが増すに従って次第に浅くなって、不純物原子は図のような分布をする。

【００８０】次に同じ端部をテーパー状にした第一マスクＭ１をマスクとしてｎ型不純物となるイオン例えばＮイオン４ａを注入する［同図（ｄ）］。これはｎ$^+$ ソース領域９３形成のためであり、加速電圧は１００ｋｅＶ、ドーズ量は約$5\times10^{15}cm^{-2}$である。加速電圧を低くしているので、注入される領域がｐ型不純物の注入領域と異なっている。

【００８１】第一マスクＭ１を除去した後、全面にＮイオン４ａを注入をする。［同図（ｅ）］。これはｎドリフト層９１ｂの表面層のｎチャネル領域の不純物濃度制御のためであり、加速電圧は２００ｋｅＶ、ドーズ量は約$1\times10^{12}cm^{-2}$である。これにより、例えばしきい値が制御できる。これ以降は、図１０（ａ）以降の注入した不純物の活性化、電極の形成等をおこなう。

【００８２】この方法を取れば、第三マスクＭ３をバックエッチして第一マスクＭ１としたので、マスク材料を改めて形成する必要がない。そして、テーパー部の角度も均一になって、ｐベース領域９２とｎソース領域９３との間隔が規定されるため、両者が整合しており、位置ずれ等のマスク合わせによる不均一の問題が起こり得ない。そして、チャネル長が均一に精度よく形成され、安定した特性が歩留まりよく得られる。

【００８３】製造方法としては、幾つかの変形も考えられる。例えばｐベース領域形成のためのｐ型不純物イオンの注入［図１２（ｃ）］と、ｎソース領域形成のためのｎ型不純物イオンの注入［図１２（ｄ）］とは逆の順序でもよく、ｎチャネル領域の不純物濃度制御のためのイオン注入［図１２（ｅ）］は最初におこなってもよい。

【００８４】

【発明の効果】以上説明したように本発明によれば、炭化けい素縦型ＦＥＴの製造方法において、第一のマスクと一部重複する第二のマスクとを用いて第一のマスクの

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一部の一方の端により第一導電型不純物導入領域を規定し、第一のマスクの一部および第二のマスクを除去して第一のマスクの別の部分により第二導電型不純物導入領域を規定することによって、第一導電型不純物導入領域および第二導電型不純物導入領域が自己整合的に形成される。

【００８５】特に端部をテーパー状にしたマスクを用い、加速電圧を変えてイオン注入する方法を取れば、一枚のマスクだけで、第一導電型不純物導入領域および第二導電型不純物導入領域を自己整合的に形成することができる。チャネル領域の不純物濃度を制御することによって、しきい電圧を制御することができ、また、ノーマリオフのＦＥＴとすることができる。

【００８６】このようにして、従来極めて困難であった非常に精密なチャネル領域をもつＪＦＥＴおよびＭＯＳＦＥＴが実現できるようになり、オン抵抗の低減に効果をもたらした。本発明は、個別のＦＥＴに限らず、ＣＭＯＳ－ＩＣや他のＳｉＣ半導体装置にも極めて有効な方法であり、高耐圧の炭化けい素半導体装置の製造を容易にするものである。

【図面の簡単な説明】

【図１】本発明第一の実施例のＭＯＳＦＥＴの部分断面図

【図２】（ａ）～（ｆ）は実施例１のＪＦＥＴの製造方法を説明するための工程順の部分断面図

【図３】（ａ）～（ｄ）は図２（ｆ）に続く実施例１のＪＦＥＴの工程順の部分断面図

【図４】実施例２のＪＦＥＴの部分断面図

【図５】実施例３のＪＦＥＴの部分断面図

【図６】実施例４のＭＯＳＦＥＴの部分断面図

【図７】（ａ）～（ｅ）は実施例４のＭＯＳＦＥＴの製造方法を説明するための工程順の部分断面図

【図８】（ａ）～（ｄ）は図７（ｅ）に続く実施例３のＭＯＳＦＥＴの工程順の部分断面図

【図９】実施例５のＭＯＳＦＥＴの部分断面図

【図１０】（ａ）～（ｅ）は実施例５のＭＯＳＦＥＴの製造方法を説明するための工程順の部分断面図

【図１１】（ａ）～（ｅ）は図１０（ｅ）に続く実施例５のＭＯＳＦＥＴの工程順の部分断面図

【図１２】（ａ）～（ｅ）は実施例６のＭＯＳＦＥＴの製造方法を説明するための工程順の部分断面図

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【図１３】従来のＪＦＥＴの部分断面図

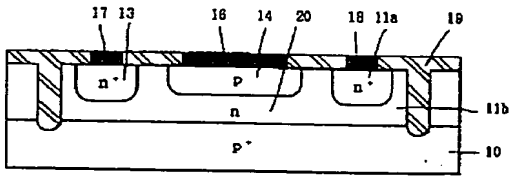
【図１４】従来のＭＯＳＦＥＴの部分断面図

【図１５】従来の別のＭＯＳＦＥＴの部分断面図

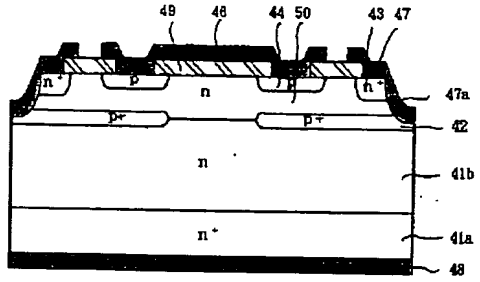
【符号の説明】

Ｍ１、Ｍ１ａ、Ｍ１ｂ　第一マスク
Ｍ２　第二マスク
Ｍ３　第三マスク
１　多結晶シリコン膜
２　SiO_2 膜
３　絶縁膜
４ａ　窒素イオン
４ｂ　窒素原子
５ａ　ほう素イオン
５ｂ　ほう素原子
６　熱酸化膜
７　凹部
８　テーパー部
９　サイドウォール
１０　ｐ型基板
１１ａ　n^+ ドレイン領域
１１ｂ、２１ｂ、３１ｂ、４１ｂ、５１ｂ、６１ｂ、７１ｂ、８１ｂ　ｎドリフト層
１３、２３、３３、４３、５３、６３、７３、８３　n^+ ソース領域
１４、４４、５４、６４　ｐゲート領域
１６、４６、６６　ゲート電極
１７、２７、３７、４７、５７、６７、７７、８７　ソース電極
１８、２８、３８、７８、８８　ドレイン電極
１９、３９、４９、５９、６９、７９、８９　絶縁膜
２０、３０、４０、５０、６０、７０、８０、９０　チャネル領域
２１ａ、３１ａ、４１ａ、７１ａ、８１ａ　n^+ ドレイン層
２２、４２、５２、７２　p^+ 埋め込み領域
２５、３５、７５、８５　ゲート酸化膜
２６、３６、７６、８６　ゲート電極層
３２、８２　ｐベース領域
３７ａ、４７ａ、７７ａ、８７ａ　凹部
５２ａ、８２ａ　p^+ コンタクト領域

【図１３】

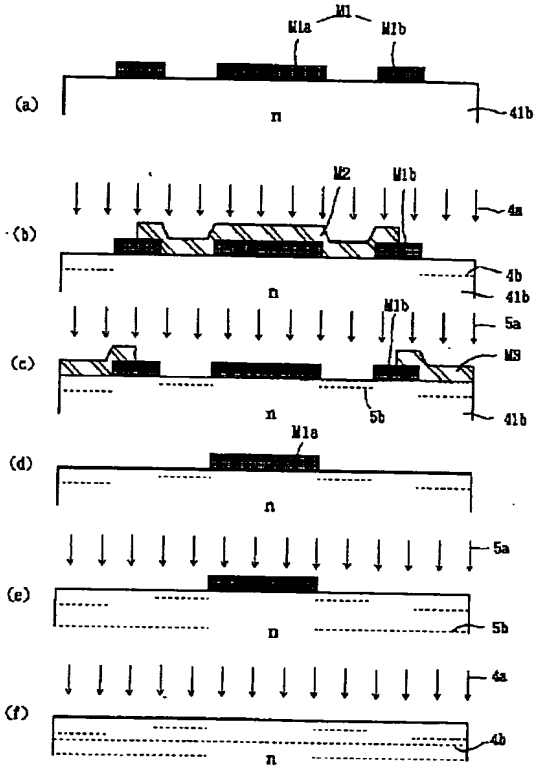


【図１】



41a n⁺ ドレイン層　　47 ソース電極
41b n ドリフト層　　47a 凹部
42 p⁺ 埋め込み領域　　48 ドレイン電極
43 n⁺ ソース領域　　49 絶縁膜
44 p ゲート領域　　50 n チャネル領域
46 ゲート電極

【図２】



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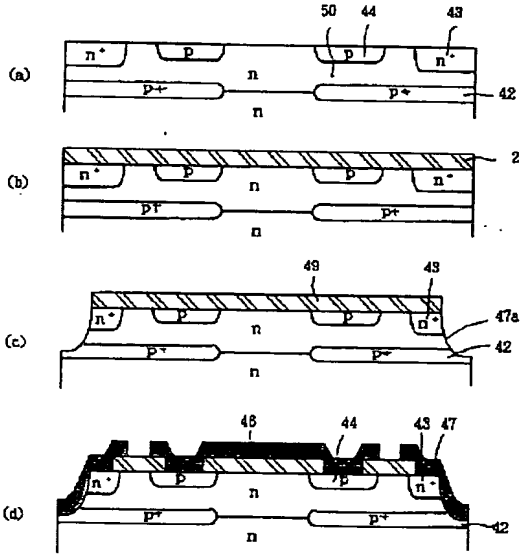
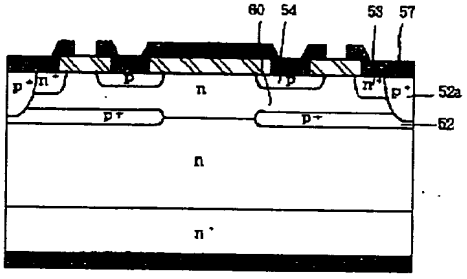


【図４】



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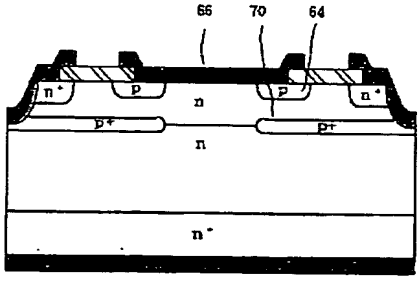

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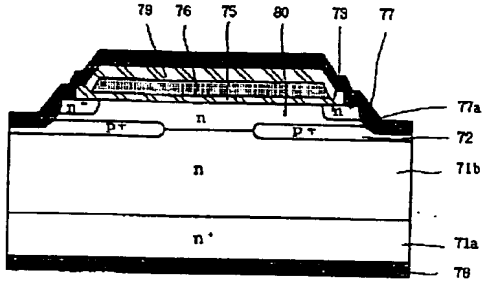

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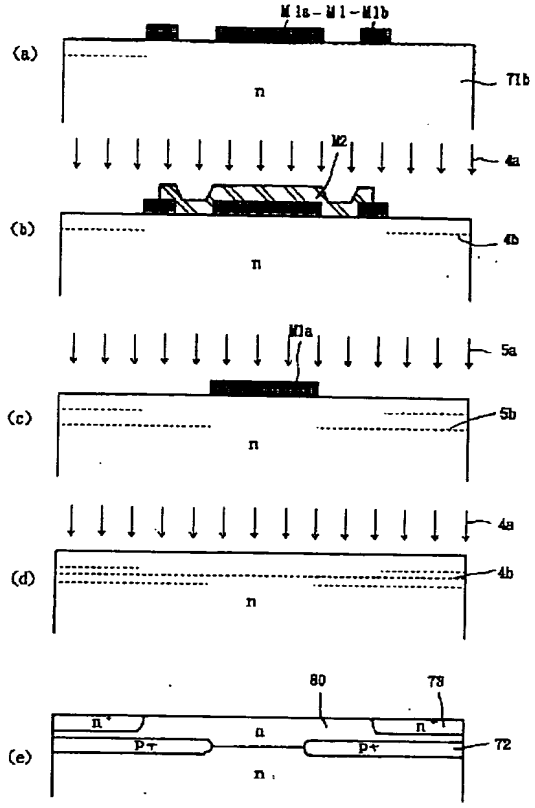

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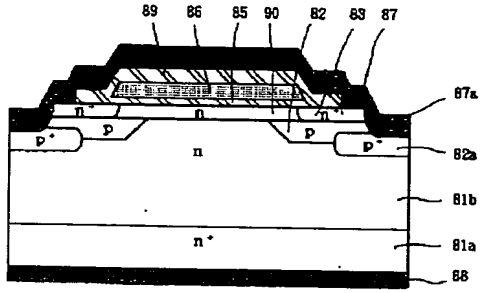
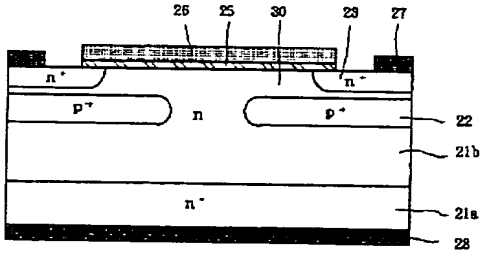


【図１４】



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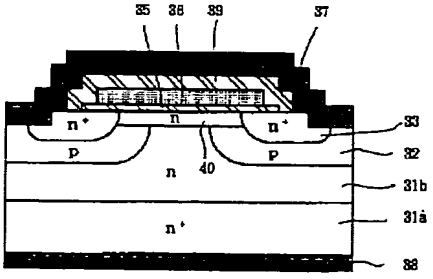

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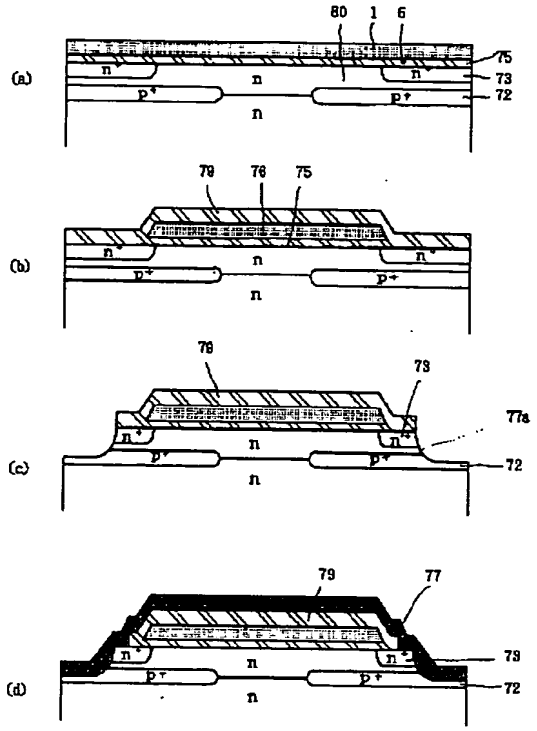
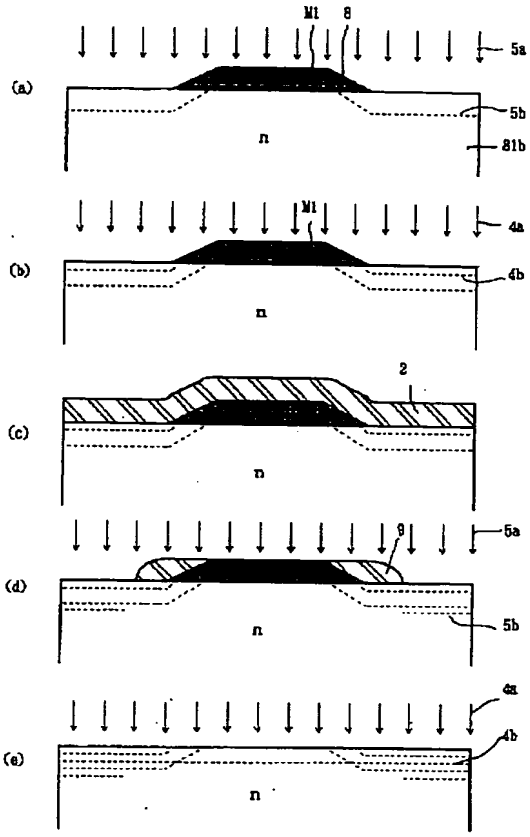
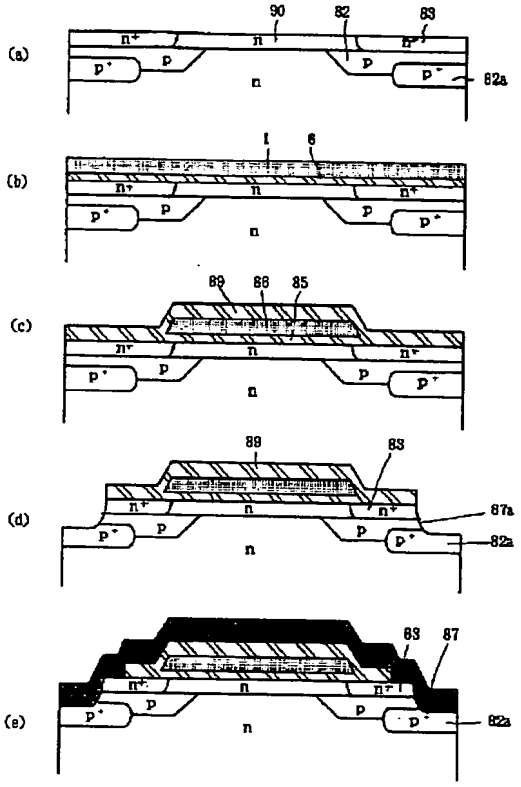

(a)
(b)
(c)
(d)
80
1
6
75
73
72
79
76
75
78
73
77a
72
79
77
73
72
n
n+
p+

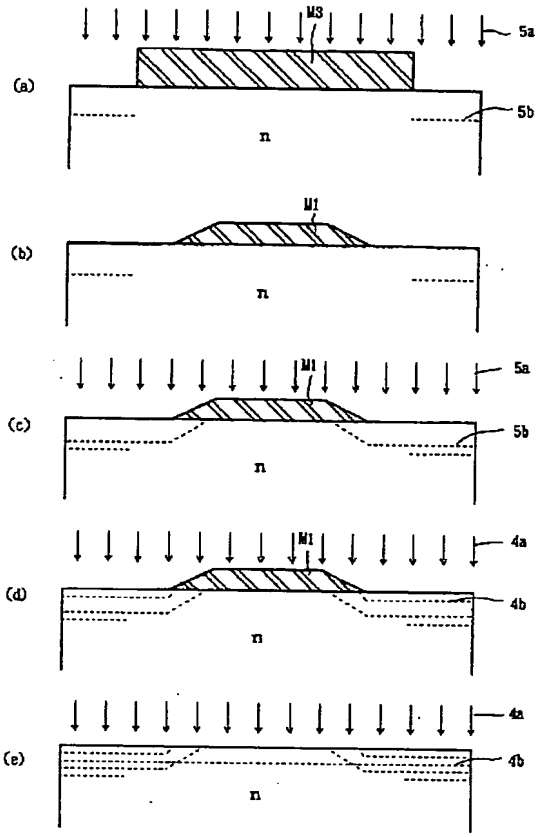
【図１０】


(a)
(b)
(c)
(d)
(e)
M1
8
5a
5b
81b
M1
4a
4b
2
9
5a
5b
4a
4b
n

【図１１】



【図１２】



CLAIMS

[Claim(s)]
[Claim 1] The first conductivity-type drift layer which consists of silicon carbide by which the laminating was carried out on the first conductivity-type silicon carbide substrate, The second conductivity-type gate field and the first conductivity-type source field which isolated to the surface layer of the first conductivity-type drift layer mutually alternatively, and were formed in it, The second conductivity-type embedding field alternatively formed in the lower part of the second conductivity-type gate field and the first conductivity-type source field, The gate electrode layer contacted and prepared in the front face of the second conductivity-type gate field, In the manufacture approach of the end-fire array FET which has the source electrode which contacted the front face of the first conductivity-type source field and the second conductivity-type embedding field in common, and was prepared in it, and the drain electrode prepared in the rear face of a silicon carbide substrate Some of one [of the first mask] edges prescribe one edge of the first conductivity-type source field. The manufacture approach of the silicon carbide end-fire array FET characterized by for some other ends of the first mask and other parts of the first mask prescribing the second conductivity-type gate field, and for other parts of said first mask prescribing the edge of the second conductivity-type embedding field, and forming each field.
[Claim 2] The process at which the first conductivity-type drift layer which consists of silicon carbide on the first conductivity-type silicon carbide substrate forms the first mask on the front face of the first conductivity-type drift layer using the substrate in which the laminating was carried out by epitaxial growth, The process which forms the second mask which consists of an ingredient which is different from the first mask so that the first mask and part may overlap, The process which introduces the impurity for the first conductivity-type source field formation into the surface layer of the first conductivity-type drift layer alternatively with those masks, The process which forms the third mask which consists of a process which removes the second mask, and an ingredient which is different from the first mask so that the first mask and part may overlap, The process which introduces the impurity for the second conductivity-type gate field formation into the surface layer of the first conductivity-type drift layer alternatively with those masks, The process which leaves a part of first mask and removes the first mask and the third mask, The process which introduces the impurity for the second conductivity-type embedding field formation into the surface layer of the first conductivity-type drift layer alternatively with the mask, The heat treatment process for activating the introduced impurity, and the process which forms the fourth mask in a silicon carbide substrate front face, The process which forms the crevice which arrives at the second conductivity-type embedding field from the front face of the first conductivity-type source field with the mask, The manufacture approach of the silicon carbide end-fire array FET which consists of the process which forms the fifth mask which

consists of an insulating material, a process which vapor-deposits a metal membrane, and a process which forms the gate electrode which consists of the metal membrane, a source electrode, and a drain electrode.

[Claim 3] The process at which the first conductivity-type drift layer which consists of silicon carbide on the first conductivity-type silicon carbide substrate forms the first mask on the front face of the first conductivity-type drift layer using the substrate in which the laminating was carried out by epitaxial growth, The process which forms the second mask which consists of an ingredient which is different from the first mask so that the first mask and part may overlap, The process which introduces the impurity for the first conductivity-type source field formation into the surface layer of the first conductivity-type drift layer alternatively with those masks, The process which forms the third mask which consists of a process which removes the second mask, and an ingredient which is different from the first mask so that the first mask and part may overlap, The process which introduces the impurity for the second conductivity-type gate field formation into the surface layer of the first conductivity-type drift layer alternatively with those masks, The process which leaves a part of first mask and removes the first mask and the third mask, The process which introduces the impurity for the second conductivity-type embedding field formation into the surface layer of the first conductivity-type drift layer alternatively with the mask, The process which forms the fourth mask in a silicon carbide substrate front face, and the process which introduces the impurity for the second conductivity-type contact field formation which arrives at the second conductivity-type embedding field with the mask, The manufacture approach of the silicon carbide end-fire array FET which consists of the heat treatment process for activating the introduced impurity, the process which forms the fifth mask which consists of an insulating material, a process which vapor-deposits a metal membrane, and a process which forms the gate electrode which consists of the metal membrane, a source electrode, and a drain electrode.

[Claim 4] The manufacture approach of the silicon carbide end-fire array FET according to claim 2 or 3 characterized by performing each installation of the impurity for the first conductivity-type source field, the second conductivity-type gate field, and the second conductivity-type embedding field formation by the ion implantation.

[Claim 5] The manufacture approach of the silicon carbide end-fire array FET according to claim 1 to 4 characterized by preparing the electrode which forms the front face and the Schottky barrier of the first conductivity-type drift layer.

[Claim 6] The first conductivity-type drift layer which consists of silicon carbide by which the laminating was carried out on the first conductivity-type silicon carbide substrate, The first conductivity-type source field alternatively formed in the surface layer of the first conductivity-type drift layer, The second conductivity-type embedding field alternatively formed in the lower part of the first conductivity-type source field, The gate electrode layer prepared through gate dielectric film on the front face of the first conductivity-type drift layer, In the manufacture approach of the end-fire array FET which has the source electrode which contacted the front face of the first conductivity-type source field and the second conductivity-type embedding field in common, and was prepared in it, and the drain electrode prepared in the rear face of a silicon carbide substrate The manufacture approach of the silicon carbide end-fire array FET characterized by specifying one edge of the first conductivity-type source field with a part of first mask, and specifying the edge of the second conductivity-type embedding field by other parts of said first mask.

[Claim 7] The process at which the first conductivity-type drift layer which consists of silicon

carbide on the first conductivity-type silicon carbide substrate forms the first mask on the front face of the first conductivity-type drift layer using the substrate in which the laminating was carried out by epitaxial growth, The process which forms the second mask which consists of an ingredient which is different from the first mask so that the first mask and part may overlap, The process which introduces the impurity for the first conductivity-type source field formation into the surface layer of the first conductivity-type drift layer alternatively with those masks, The process which leaves a part of first mask and removes the first mask and the second mask, The process which introduces the impurity for the second conductivity-type embedding field formation into the surface layer of the first conductivity-type drift layer alternatively with those masks, The process which removes a part of first mask which it left, and the heat treatment process for activating the introduced impurity, The process which forms gate oxide in a silicon carbide substrate front face by thermal oxidation, The process which carries out pattern formation after depositing a polycrystalline silicon layer on the gate oxide, The process which forms the third mask after covering an insulator layer, and the process which forms the crevice which arrives at the second conductivity-type embedding field from the front face of the first conductivity-type source field with the mask, The gate electrode which serves as a process which prepares the aperture for contact in an insulator layer, and vapor-deposits a metal membrane from the metal membrane, and contacts a polycrystalline silicon layer, The manufacture approach of the silicon carbide end-fire array FET which consists of a process which forms the source electrode in contact with the first conductivity-type source field and the second conductivity-type contact field, and the drain electrode in contact with a silicon carbide substrate.

[Claim 8] The process at which the first conductivity-type drift layer which consists of silicon carbide on the first conductivity-type silicon carbide substrate forms the first mask on the front face of the first conductivity-type drift layer using the substrate in which the laminating was carried out by epitaxial growth, The process which forms the second mask which consists of an ingredient which is different from the first mask so that the first mask and part may overlap, The process which introduces the impurity for the first conductivity-type source field formation into the surface layer of the first conductivity-type drift layer alternatively with those masks, The process which leaves a part of first mask and removes the first mask and the second mask, The process which introduces the impurity for the second conductivity-type embedding field formation into the surface layer of the first conductivity-type drift layer alternatively with those masks, The process which forms the third mask in a silicon carbide substrate front face, and the process which introduces the impurity for the second conductivity-type contact field formation which arrives at the second conductivity-type embedding field with the mask, The heat treatment process for activating the introduced impurity, and the process which forms gate oxide in a silicon carbide substrate front face by thermal oxidation, The process which carries out pattern formation after depositing a polycrystalline silicon layer on the gate oxide, The process which covers an insulator layer, and the process which prepares the aperture for contact in the insulator layer, and vapor-deposits a metal membrane, The manufacture approach of the silicon carbide end-fire array FET which consists of a process which forms the gate electrode which consists of the metal membrane and contacts a polycrystalline silicon layer, the source electrode in contact with the first conductivity-type source field and the second conductivity-type contact field, and the drain electrode in contact with a silicon carbide substrate.

[Claim 9] The first conductivity-type drift layer which consists of silicon carbide by which the laminating was carried out on the first conductivity-type silicon carbide substrate, The first conductivity-type source field alternatively formed in the surface layer of the first conductivity-

type drift layer, The second conductivity-type base region alternatively formed in the lower part of the first conductivity-type source field, The gate electrode layer prepared through gate dielectric film on the front face of the first conductivity-type drift layer, In the manufacture approach of the end-fire array FET which has the source electrode which contacted the front face of the first conductivity-type source field and the second conductivity-type base region in common, and was prepared in it, and the drain electrode prepared in the rear face of a silicon carbide substrate The manufacture approach of the silicon carbide end-fire array FET characterized by for a part with the thick thickness of the first mask of the shape of a taper with a loose edge prescribing one edge of the first conductivity-type source field, and specifying the edge of the second conductivity-type base region by the part with the thin thickness of the first mask of said first mask.

[Claim 10] The substrate with which the laminating of the first conductivity-type drift layer which consists of silicon carbide on the first conductivity-type silicon carbide substrate was carried out by epitaxial growth is used. The process which forms the first mask of the shape of a taper with a loose edge on the front face of the first conductivity-type drift layer, The process which introduces the impurity for the second conductivity-type base region formation into the surface layer of the first conductivity-type drift layer alternatively by the part with the thick thickness of the mask, The process which introduces the impurity for the first conductivity-type source field formation into the surface layer of the first conductivity-type drift layer alternatively by the part with the thin thickness of the first mask, The process which forms the third mask in a silicon carbide substrate front face, and the process which introduces the impurity for the second conductivity-type contact field formation which arrives at the second conductivity-type base region with the mask, The heat treatment process for activating the introduced impurity, and the process which forms gate oxide in a silicon carbide substrate front face by thermal oxidation, The process which carries out pattern formation after depositing a polycrystalline silicon layer on the gate oxide, The gate electrode which serves as a process which prepares the aperture for contact and vapor-deposits a metal membrane after covering an insulator layer from the metal membrane, and contacts a polycrystalline silicon layer, The manufacture approach of the silicon carbide end-fire array FET which consists of a process which forms the source electrode in contact with the first conductivity-type source field and the second conductivity-type contact field, and the drain electrode in contact with a silicon carbide substrate.

[Claim 11] The substrate with which the laminating of the first conductivity-type drift layer which consists of silicon carbide on the first conductivity-type silicon carbide substrate was carried out by epitaxial growth is used. The process which forms the first mask of the shape of a taper with a loose edge on the front face of the first conductivity-type drift layer, The process which introduces the impurity for the first conductivity-type source field formation into the surface layer of the first conductivity-type drift layer alternatively by the part with the thick thickness of the mask, The process which introduces the impurity for the second conductivity-type base region formation into the surface layer of the first conductivity-type drift layer alternatively by the part with the thick thickness of the first mask, The process which forms the third mask in a silicon carbide substrate front face, and the process which introduces the impurity for the second conductivity-type contact field formation which arrives at the second conductivity-type base region with the mask, The process which removes the first mask, and the heat treatment process for activating the introduced impurity, The process which forms gate oxide in a silicon carbide substrate front face by thermal oxidation, The process which carries out pattern formation after depositing a polycrystalline silicon layer on the gate oxide, The process

which forms the third mask after covering an insulator layer, and the process which forms the crevice which arrives at the second conductivity-type contact field from the front face of the first conductivity-type source field with the mask, The gate electrode which serves as a process which prepares the aperture for contact in an insulator layer, and vapor-deposits a metal membrane from the metal membrane, and contacts a polycrystalline silicon layer, The manufacture approach of the silicon carbide end-fire array FET which consists of a process which forms the source electrode in contact with the first conductivity-type source field and the second conductivity-type contact field, and the drain electrode in contact with a silicon carbide substrate.
[Claim 12] The manufacture approach of the silicon carbide end-fire array FET according to claim 10 or 11 characterized by preparing a sidewall in the side of the first mask and using the first mask and its sidewall as the third mask.
[Claim 13] The manufacture approach of the silicon carbide end-fire array FET according to claim 9 to 11 characterized by carrying out etchback of the third mask, and an edge considering as the first mask of the shape of a loose taper after passing through the process which forms the third mask with the thick thickness for the second conductivity-type contact field formation which arrives at the second conductivity-type base region, and the process which introduces an impurity with the mask previously.
[Claim 14] The manufacture approach of the silicon carbide end-fire array FET according to claim 6 to 13 characterized by performing each installation of the impurity for the first conductivity-type source field, the second conductivity-type embedding field, and the second conductivity-type base region formation by the ion implantation.
[Claim 15] The manufacture approach of the silicon carbide end-fire array FET according to claim 1 to 14 characterized by adding the process which introduces the first conductivity-type impurity for high-impurity-concentration control of a channel field into the whole surface of the surface layer of the first conductivity-type drift layer.
[Claim 16] The first conductivity-type drift layer which consists of silicon carbide by which the laminating was carried out on the first conductivity-type silicon carbide substrate, The second conductivity-type base region where at least the part was alternatively embedded and formed in the surface layer of the first conductivity-type drift layer, The first conductivity-type source field formed in a part of upper part of the second conductivity-type base region in contact with the second conductivity-type base region, The gate electrode layer prepared through gate dielectric film on the channel field which is the first conductivity-type drift layer left behind on the second conductivity-type base region, In the end-fire array FET which has the source electrode which contacted the front face of the first conductivity-type source field and the second conductivity-type base region in common, and was prepared in it, and the drain electrode prepared in the rear face of a silicon carbide substrate Silicon carbide end-fire array FET characterized by becoming shallow almost linearly, so that the junction depth of the edge of the second conductivity-type base region keeps away from the first conductivity-type source field.
[Claim 17] Silicon carbide end-fire array FET according to claim 16 characterized by preparing the second conductivity-type contact field where the junction depth is deeper than the second conductivity-type base region, and a source electrode touching the front face of the second conductivity-type contact field with high high impurity concentration from the second conductivity-type base region so that a part may overlap the second conductivity-type base region.
[Claim 18] Silicon carbide end-fire array FET according to claim 16 characterized by embedding the second conductivity-type contact field, being prepared, preparing the crevice which arrives at

the second conductivity-type contact field from the front face of the first conductivity-type source field, and a source electrode touching the exposure front face of the second conductivity-type contact field.

[Claim 19] Silicon carbide end-fire array FET according to claim 16 to 18 to which high impurity concentration of a channel field is characterized by being high concentration from that of the first conductivity-type drift layer.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the manufacture approach of a vertical mold field-effect transistor (it is described as Following FET) and the vertical mold electric field effect FET with the gate of the assembling die which used silicon carbide as a semiconductor material and which is a power semiconductor device, or the MOS mold of metal-oxide film-semi-conductor structure.
[0002]
[Description of the Prior Art] Since a band gap is large and the maximum insulation electric field are large a figure single [about] as compared with silicon (it is described as Following Si), silicon carbide (it is described as Following SiC) is an ingredient with which the application to a next-generation power semiconductor device is expected. It is applied to various electron devices until now using the single crystal wafer called 4 H-SiC or 6 H-SiC, and it is thought that it is especially suitable for an elevated temperature and the component for large power. The above-mentioned crystal is the alpha phase SiC of the form which carried out the laminating of a sphalerite mold and the wurtzite mold. The semiconductor device is made also for the crystal of the beta phase SiC otherwise called 3 C-SiC as an experiment. [, for example, Weitzel, by which CMOS-IC which is the general-purpose semiconductor devices, such as schottky diode, end-fire array MOSFET, and a thyristor, as a component for power is recently made as an experiment, and it is checked from the property as compared with the conventional Si semiconductor device that a property is very good, :IEEE Trans.on Electron Devices besides C.W., and vol. -- 43, No.10, and pp.1732-1741 --] (1997) . Some examples of MOSFET are shown below.
[0003] Drawing 13 is the fragmentary sectional view of the unit cell of junction type FET (it omits Following JFET) currently developed as one of the RF components [and Abstracta of Int.Conf.on Silicon Carbide besides Sheppard and S.T., III-Nitrides and Related Materials] (1997). p+ It is n+ to the surface layer of n drift layer 11 by which the laminating was carried out on the substrate 10. The source field 13, p gate field 15, and n+ The drain field is formed. n+ The source field 13 and n+ The drain field 14 and p gate field 15 are contacted, and the source electrode 17, the drain electrode 18, and the gate electrode 16 are formed, respectively.
[0004] When an electrical potential difference is impressed to the gate electrode 16 with this structure, they are p gate field 15 to p gate field 15, and p+. A depletion layer spreads to the n channel field 20 between substrates 10. The current between the source electrode 17 and the drain electrode 18 is controlled by this. Moreover, a current flows again between the drain electrode 18 and the source electrode 17 by removing the electrical potential difference impressed to the gate electrode 16. Thus, the current between source drains serves as a component switchable [with gate voltage]. Since this JFET depletion-izes a channel field by

electrical-potential-difference impression to the gate electrode 16, it is called a depletion type. A front face to p+ The slot which reaches a substrate 10 is formed and it fills up with the insulator layer 19 because [of isolation].

[0005] On the other hand, drawing 14 is one sort of a vertical mold MOSFET [Shenoy, J.N. others , Abstracta of Int.Conf.on Silicon Carbide, III-Nitrides and Related Materials] (1997). n+ It is p+ by the ion implantation of high acceleration voltage [surface layer / of n drift layer 21b by which the laminating was carried out on substrate 21a]. The embedding field 22 is formed. The p+ It is n+ to the surface layer of n drift layer part 21b on the embedding field 22. The source field 23 is formed. Two n+ The gate electrode 26 is formed through gate dielectric film 25 on the front face of n drift layer part 21b inserted into the source field 23. n+ The source electrode 27 is n+ to the front face of the source field 23. The drain electrode 28 is formed in the rear face of substrate 21a, respectively.

[0006] In this example, the gate part has metal-oxide-semiconductor structure which impresses an electrical potential difference through gate dielectric film 25 instead of pn junction. In this MOSFET, by impressing a forward electrical potential difference to the gate electrode layer 26, induction of the accumulation layer is carried out to the n channel field 30 of the surface part of n drift layer 21b of gate electrode 26 directly under, and a current flows between the drain electrode 28 and the source electrode 27. Moreover, if a negative electrical potential difference is impressed to the gate electrode 26, the current between the drain electrode 28 and the source electrode 27 can be intercepted, and it has a switching function. The electrical potential difference between source drains is p+. It is possible for it to be impressed between the embedding field 22 and n drift layer 21b, and to hold a big electrical potential difference, and it is made the structure suitable for high pressure-proofing. Since this MOSFET forms an accumulation layer by electrical-potential-difference impression to the gate electrode 26, it is called ACCUFET.

[0007] Drawing 15 is [and Phys.Stat.Sol. (a) besides Onda and S., vol.162, and p.369] (1997) which are the fragmentary sectional view of the unit cell of another vertical mold quantity proof-pressure MOSFET **. . n+ The p base region 32 is formed on substrate 31a at the surface layer of n drift layer 31b by which the laminating was carried out, and it is n+ to the surface layer of the p base region 32. The source field 33 is formed. Two n+ The n channel field 40 which connects the source field 33 is formed of epitaxial growth, and the gate electrode layer 36 is formed through gate dielectric film 35 on the front face of the n channel field 40. n+ The source electrode 27 is n+ to the front face of the source field 33. The drain electrode 38 is formed in the rear face of substrate 31a, respectively.

[0008] By impressing a forward electrical potential difference to the gate electrode layer 36 also in this case, induction of the accumulation layer is carried out to the surface part of the n channel field 40 of gate electrode layer 36 directly under, and it becomes possible to pass the current from the drain electrode 38 to the source electrode 37. Moreover, between the drain electrode 38 and the source electrodes 27 will be intercepted, and by impressing a negative electrical potential difference to the gate electrode layer 36 will show a switching function.

[0009] Otherwise, although there is also an example of a prototype of MOSFET of a planar mold or a trench mold, by SiC, that the mobility of an inversion layer is very small gets down that it is experimentally sudden, and it is thought that FET of the enhancement type using an inversion layer is not suitable for practical use. It is the example of the structure where have the common description in that it is not FET of the enhancement type with which the component of the three above-mentioned examples uses an inversion layer to it but FET using the semi-conductor layer

of a conductivity type from the first as a channel, especially it is suitable for SiC.
[0010]
[Problem(s) to be Solved by the Invention] When it is going to manufacture the semiconductor device for power, the actual former not much good property is not realized, or the structure of drawing 13 , and 14 or drawing 15 is not manufactured in fact, although the property which was very excellent is expected. It is the double diffusion MOS (D-MOS) whose one of the reason of the is an approach which has spread most with Si semi-conductor. Structure is in an easily unrealizable point in SiC. In Si, a precise channel consistency is realized by introducing p mold impurity and n mold impurity alternatively with the same mask, and carrying out thermal diffusion. Namely, the dimension of the channel which influences the property of MOSFET is very controllable to a precision, and can make MOSFET with the sufficient yield.
[0011] It receives that can come and it is alike, and by SiC, the rate of activation of the impurity which carried out the ion implantation is bad, in order to raise this, an ion implantation 1000 degrees C or more and heat-of-activation processing at 1600 degrees C or more are required, and the diffusion of an impurity which carried out the ion implantation hardly breaks out. Therefore, installation of p mold impurity and n mold impurity must be depended on a respectively separate mask, and control of a precise channel consistency is not realized. Therefore, it becomes the thing also with the very big variation which has large channel resistance, and resistance of the whole component is like [as which it will be mostly specified by channel resistance]. It can be said that the property of SiC original is not acquired.
[0012] In view of the above problem, the purpose of this invention can realize a very precise channel, and is to offer the manufacture approach of silicon carbide vertical FET and silicon carbide vertical FET which can be high-pressure=proofed easily.
[0013]
[Means for Solving the Problem] The first conductivity-type drift layer which this invention becomes from the silicon carbide by which the laminating was carried out on the first conductivity-type silicon carbide substrate for the above-mentioned technical-problem solution, The second conductivity-type gate field and the first conductivity-type source field which isolated to the surface layer of the first conductivity-type drift layer mutually alternatively, and were formed in it, The second conductivity-type embedding field alternatively formed in the lower part of the second conductivity-type gate field and the first conductivity-type source field, The gate electrode layer contacted and prepared in the front face of the second conductivity-type gate field, In the manufacture approach of the end-fire array FET which has the source electrode which contacted the front face of the first conductivity-type source field and the second conductivity-type embedding field in common, and was prepared in it, and the drain electrode prepared in the rear face of a silicon carbide substrate some of one [of the first mask] edges -- one edge of the first conductivity-type source field -- specifying -- some other ends of the first mask, and other parts of the first mask -- the second conductivity-type gate field -- ** -- probably -- ** -- Other parts of said first mask shall prescribe the edge of the second conductivity-type embedding field.
[0014] For example, the substrate with which the laminating of the first conductivity-type drift layer which consists of silicon carbide on the first conductivity-type silicon carbide substrate was carried out by epitaxial growth as a concrete process is used. The process which forms the first mask on the front face of the first conductivity-type drift layer, The process which forms the second mask which consists of an ingredient which is different from the first mask so that the first mask and part may overlap, The process which introduces the impurity for the first

conductivity-type source field formation into the surface layer of the first conductivity-type drift layer alternatively with those masks, The process which forms the third mask which consists of a process which removes the second mask, and an ingredient which is different from the first mask so that the first mask and part may overlap, The process which introduces the impurity for the second conductivity-type gate field formation into the surface layer of the first conductivity-type drift layer alternatively with those masks, The process which leaves a part of first mask and removes the first mask and the third mask, The process which introduces the impurity for the second conductivity-type embedding field formation into the surface layer of the first conductivity-type drift layer alternatively with the mask, The heat treatment process for activating the introduced impurity, and the process which forms the fourth mask in a silicon carbide substrate front face, The process which forms the crevice which arrives at the second conductivity-type embedding field from the front face of the first conductivity-type source field with the mask, It shall consist of the process which forms the fifth mask which consists of an insulating material, a process which vapor-deposits a metal membrane, and a process which forms the gate electrode which consists of the metal membrane, a source electrode, and a drain electrode.

[0015] If it is made such, since the substantial dimension of a channel field is decided in the second conductivity-type gate field, the ununiformity by mask alignment will be avoided and precise control will be attained. It is possible for this to manufacture small FET of on resistance. Instead of forming the crevice which arrives at the second conductivity-type embedding field from the front face of the first conductivity-type source field, and preparing a source electrode, the second conductivity-type contact field which arrives at the second conductivity-type embedding field may be formed. If it is made such, a source electrode can be prepared on a front face.

[0016] Also in the thing to which each installation of the impurity for the first conductivity-type source field, the second conductivity-type gate field, and the second conductivity-type embedding field formation is especially performed by the ion implantation, then SiC, formation of an impurity range can be performed certainly. The electrode which forms the front face and the Schottky barrier of the first conductivity-type drift layer may be prepared.

[0017] If it is made such, it can consider as a channel field smaller than the dimension of the second conductivity-type gate field required for contact resistance. Moreover, the first conductivity-type drift layer which consists of silicon carbide by which the laminating was carried out on the first conductivity-type silicon carbide substrate, The first conductivity-type source field alternatively formed in the surface layer of the first conductivity-type drift layer, The second conductivity-type embedding field alternatively formed in the lower part of the first conductivity-type source field, The gate electrode layer prepared through gate dielectric film on the front face of the first conductivity-type drift layer, In the manufacture approach of the end-fire array FET which has the source electrode which contacted the front face of the first conductivity-type source field and the second conductivity-type embedding field in common, and was prepared in it, and the drain electrode prepared in the rear face of a silicon carbide substrate One edge of the first conductivity-type source field shall be specified with a part of first mask, and other parts of said first mask shall prescribe the edge of the second conductivity-type embedding field.

[0018] For example, the substrate with which the laminating of the first conductivity-type drift layer which consists of silicon carbide on the first conductivity-type silicon carbide substrate was carried out by epitaxial growth as a concrete process is used. The process which forms the first

mask on the front face of the first conductivity-type drift layer, The process which forms the second mask which consists of an ingredient which is different from the first mask so that the first mask and part may overlap, The process which introduces the impurity for the first conductivity-type source field formation into the surface layer of the first conductivity-type drift layer alternatively with those masks, The process which leaves a part of first mask and removes the first mask and the second mask, The process which introduces the impurity for the second conductivity-type embedding field formation into the surface layer of the first conductivity-type drift layer alternatively with those masks, The process which removes a part of first mask which it left, and the heat treatment process for activating the introduced impurity, The process which forms gate oxide in a silicon carbide substrate front face by thermal oxidation, The process which carries out pattern formation after depositing a polycrystalline silicon layer on the gate oxide, The process which forms the third mask after covering an insulator layer, and the process which forms the crevice which arrives at the second conductivity-type embedding field from the front face of the first conductivity-type source field with the mask, It shall consist of a process which prepares the aperture for contact in an insulator layer, and vapor-deposits a metal membrane, and a process which forms the gate electrode which consists of the metal membrane, a source electrode, and a drain electrode.

[0019] Since the dimension of a channel field is decided with the first mask also in this case, the ununiformity by mask alignment is avoided and precise control is attained. Instead of forming the crevice which arrives at the second conductivity-type embedding field from the front face of the first conductivity-type source field, and preparing a source electrode, the second conductivity-type contact field which arrives at the second conductivity-type embedding field may be formed. If it is made such, a source electrode can be prepared on a front face.

[0020] A part with the thickness of the first mask of the shape of a taper with a loose edge thick as an option can prescribe one edge of the first conductivity-type source field, and a part with the thin thickness of the first mask of said first mask can also prescribe the edge of the second conductivity-type base region. For example, the substrate with which the laminating of the first conductivity-type drift layer which consists of silicon carbide on the first conductivity-type silicon carbide substrate was carried out by epitaxial growth as a concrete process is used. The process which forms the first mask on the front face of the first conductivity-type drift layer, The process which forms the first mask of the shape of a taper with a loose edge, and the process which introduces the impurity for the first conductivity-type source field formation into the surface layer of the first conductivity-type drift layer alternatively by the part with the thick thickness of the mask, The process which introduces the impurity for the second conductivity-type base region formation into the surface layer of the first conductivity-type drift layer alternatively by the part with the thick thickness of the first mask, The process which forms the third mask in a silicon carbide substrate front face, and the process which introduces the impurity for the second conductivity-type contact field formation which arrives at the second conductivity-type base region with the mask, The process which removes the first mask, and the heat treatment process for activating the introduced impurity, The process which forms gate oxide in a silicon carbide substrate front face by thermal oxidation, It shall consist of the process which carries out pattern formation after depositing a polycrystalline silicon layer on the gate oxide, the process which covers an insulator layer, a process which prepares the aperture for contact in an insulator layer, and vapor-deposits a metal membrane, and a process which forms the gate electrode which consists of the metal membrane, a source electrode, and a drain electrode.

[0021] Since the dimension of a channel field is decided with the first mask also in this case, the ununiformity by mask alignment is avoided and precise control is attained. And another mask for impurity range formation is not needed. The crevice which arrives at the second conductivity-type base region from the front face of the first conductivity-type source field may be formed, and the source electrode in contact with the first conductivity-type source field and the second conductivity-type contact field may be prepared.
[0022] It is good to add the impurity installation process for the second conductivity-type contact field formation by using as a mask the process which prepares a sidewall in the side of the first mask especially, and the first mask and sidewall. If it is made such, it will not be based on mask alignment but formation of the second conductivity-type base region and the shifted second conductivity-type contact field can be performed.
[0023] The third mask with the thick thickness for the second conductivity-type contact field formation is formed, after passing through the process which introduces an impurity with the mask previously, etchback of the third mask can be carried out, and an edge can consider as the first mask of the shape of a loose taper. If it is made such, the first mask and third mask of a basis will be the same, and will not have the need of forming another mask ingredient.
[0024] Furthermore, also in the thing to which each installation of the impurity for the first conductivity-type source field, the second conductivity-type embedding field, and the second conductivity-type base region formation is performed by the ion implantation, then SiC, formation of an impurity range can be performed certainly. And the process which introduces the first conductivity-type impurity for high-impurity-concentration control of a channel field into the whole surface of the surface layer of the first conductivity-type drift layer shall be added.
[0025] By controlling the high impurity concentration of a channel field, threshold voltage can be controlled and it can be referred to as FET of no MARIOFU. The first conductivity-type drift layer which consists of silicon carbide by which the laminating was carried out on the first conductivity-type silicon carbide substrate by the above manufacture approaches, The second conductivity-type base region where at least the part was alternatively embedded and formed in the surface layer of the first conductivity-type drift layer, The first conductivity-type source field formed in a part of upper part of the second conductivity-type base region in contact with the second conductivity-type base region, The gate electrode layer prepared through gate dielectric film on the channel field which is the first conductivity-type drift layer left behind on the second conductivity-type base region, The source electrode which contacted the front face of the first conductivity-type source field and the second conductivity-type base region in common, and was prepared in it, If it considers as the silicon carbide end-fire array FET which becomes shallow almost linearly so that it has the drain electrode prepared in the rear face of a silicon carbide substrate and the junction depth of the edge of the second conductivity-type base region keeps away from the first conductivity-type source field Control of the die length of a channel field is easy, and the end-fire array FET with a uniform channel field can manufacture easily.
[0026] From the second conductivity-type base region, even if it prepares the second conductivity-type contact field where the junction depth is deeper than the second conductivity-type base region and contacts a source electrode on the front face of the second conductivity-type contact field with high high impurity concentration, the crevice which arrives at the second conductivity-type contact field from the front face of the first conductivity-type source field is prepared, and a source electrode may be contacted on the exposure front face of the second conductivity-type contact field, so that a part may overlap the second conductivity-type base region.

[0027] If there is no need of preparing a crevice if a source electrode is contacted on the front face of the second conductivity-type contact field on the same front face as the first conductivity-type source field, the crevice which arrives at the second conductivity-type contact field from the front face of the first conductivity-type source field is prepared and a source electrode is contacted, there will be no need of thickening thickness of the second conductivity-type contact field. By controlling the thing which is high concentration, then high impurity concentration from that of the first conductivity-type drift layer, the high impurity concentration of a channel field can control threshold voltage, and can set to FET of no MARIOFU.
[0028]
[Embodiment of the Invention] Below, this invention is explained to a detail, while an example is shown. However, explanation is omitted about drawing 13 -15, a common part, or a part without this invention or instead of. Although n channel MOS FET is taken for the example as an important application of this invention, of course, this invention can be adapted also for p channel MOS FET which made the conductivity type reverse. In addition, the silicon carbide explained here is aimed at what is mainly called 6H and 4H, although many polytypes exist as known well.
[0029] [Example 1] drawing 1 is the first example (it is described as an example 1 below.) of this invention. the following -- being the same -- it is the sectional view of the unit cell of starting SiCJFET. This supports the component which formed the conventional component of drawing 13 into high pressure-proofing. n+ It sets to the wafer with which the laminating of the n drift layer 41b was carried out by epitaxial growth on substrate 41a, and is p+ from the front face of n drift layer 41b to a somewhat deep location. The embedding field 42 is formed and it is p+. In the surface layer of upper n drift layer 41b of the embedding field 42, they are p gate field 44 and n+. The source field 43 is formed. The gate electrode 46 is formed on the front face of p gate field 44. n+ From the front face of the source field 43, the front face of investigated crevice 47a is met, and it is n+. The source field 43 and p+ It contacts common to a front face with the embedding field 42, and the source electrode 47 is formed, and it is n+. The rear face of substrate 41a is contacted and the drain electrode 48 is formed.
[0030] Examples of the main dimensions are the following values. n+ For the high impurity concentration of substrate 41a, it of 1x1018cm in 350 micrometers in 3 and thickness and n drift layer 41b is 1x1016cm 10 micrometers in 3 and thickness. p+ The highest high impurity concentration of the embedding field 42 is 5x1018cm 0.5 micrometers in 3 and thickness, and n 0.5-micrometer drift layer 41b is on it. p+ of both sides Spacing between the embedding fields 42 is about 5 micrometers. n+ The high impurity concentration of the source field 43 is 1x1019cm 3 and a junction depth of 0.2 micrometers, and width of face is [3 and a junction depth of 0.2 micrometers of 5x1018cm, and the width of face of it of about 3 micrometers and p gate field 44] about 2 micrometers. n+ Spacing between the source field 43 and p gate field 44 is about 1 micrometer, and n drift layer 41b has arrived at the front face. The depth of crevice 47a investigated from the front face is 0.7 micrometers, and width of face is about 3 micrometers. The pitch of the unit cell of drawing is about 25 micrometers.
[0031] Although the point different from the horizontal type JFET of drawing 13 is a point that the source electrode 47 and the drain electrode 48 serve as FET of the vertical mold formed in both sides of a semi-conductor substrate, the actuation is not fundamentally different from the thing of drawing 11 . That is, a depletion layer is breadth and n+ by impressing an electrical potential difference to the gate electrode 46 to the channel field 50 of p gate field 44 to a lower part. The source field 43 and n drift layer 41b are insulated electrically. As a result, the current

from the drain electrode 38 to the source electrode 37 is controlled. It is JFET same depression type as what was shown in drawing 13 .

[0032] Drawing 2 (a) thru/or (f) and drawing 3 (a) thru/or (d) are the fragmentary sectional views near the front face of the order of a production process for explaining the manufacture approach of SiCJFET of the example 1 of drawing 1 . It explains in order of below. First, n+ 4 H-SiC substrate which carried out the laminating of the n drift layer 41b of a phosphorus dope with epitaxial growth is prepared on substrate 41a. For example, the high impurity concentration of n drift layer 41b is 1x1016cm-3, and thickness is 10 micrometers. On the front face of the n drift layer 41b, the polycrystal silicone film 1 is deposited with a reduced pressure CVD method, a pattern is formed by the photolithography, and it considers as the first mask M1 [drawing 2 (a)]. The first mask M1 consists of each part of M1a of a center section, and M1b of both sides. Thickness of the polycrystal silicone film 1 was set to 1 micrometer. The first mask M1 does not necessarily need to be a polycrystal silicone film, and as long as it turns into a mask of alternative etching, it may be the oxidization silicon film (henceforth, SiO2 it is described as the film) well used for a silicon process etc., the nitriding silicon film, or a photoresist. However, to carry out an ion implantation at an elevated temperature, it is necessary to use the ingredient which ceases to the elevated temperature of polycrystalline silicon etc.

[0033] It is SiO2 by the heat CVD method on the first mask M1 of the polycrystal silicone film 1. After depositing the film 2, forming a pattern by the photolithography and considering as the second mask M2, the ion used as n mold impurity, for example, nitrogen (it is described as Following N) ion 4a, is poured into the field specified with the second mask M1 and M2 for a start [these] [this drawing (b)]. 4b is poured-in N atom. This is n+. It is for source field 43 formation, and acceleration voltage is 100keV(s) and a dose is abbreviation 5x1015cm-2. The temperature at the time of an ion implantation is about 800 degrees C. The rate of activation can be raised by carrying out an ion implantation at an elevated temperature. The second mask M2 is not necessarily SiO2. Although it is not necessary to be the film, since it is required to remove leaving the first mask M1 at a next process, it considers as a different ingredient from the first mask M1, and it can be necessary to be made to perform alternative etching. For example, when a polycrystal silicone film is used as the first mask M1, it is SiO2 like the upper example as the second mask M2. If the film is used, only the second mask 2 is removable with fluoric acid. It is SiO2 by reactive ion etching (it is described as Following RIE) the reverse is also possible and using the mixed gas of a carbon tetrachloride and oxygen etc. in that case. It is possible to control the etch rate of the film and a polycrystal silicone film, and to etch only a polycrystal silicone film. Thus, alternative removal is just performed to the first mask M1. Since the second mask M2 should just have an edge on the first mask M1, it is easy mask alignment. As an n mold impurity, phosphorus (it is described as Following P) etc. is used other than N.

[0034] SiO2 The second membranous mask M2 is removed and it is SiO2 by the heat CVD method again. After depositing the film 2, forming a pattern by the photolithography and considering as the third mask M3, the ion used as p mold impurity, for example, boron (it is described as Following B) ion 5a, is poured into the field specified with the third mask M1 and M3 for a start [these] [this drawing (c)]. 5b is poured-in B atom. This is for p gate field 44 formation, acceleration voltage is 100keV(s) and a dose is abbreviation 5x1015cm-2. Also in this case, the third mask M3 is not necessarily SiO2. It is not necessary to be the film and alternative removal is just performed to the first mask M1 at a next process. Since the third mask M3 should just have an edge on the first mask M1, it is easy mask alignment. As p mold impurity and a becoming impurity, aluminum (it is described as Following aluminum) etc. can be used other

than B.
[0035] SiO2 the third membranous mask M3 -- removing -- a photolithography -- ** -- a part of first mask -- M1b -- removing -- a part of first mask -- [this drawing (d)] which leaves M1a. a part of first mask which it left -- M1a is used as a mask and B ion 5a is poured in again. [This drawing (e)]. This is p+. It is for embedding field 42 formation, and acceleration voltage is 400keV(s) and a dose is abbreviation 1x1015cm-2. Acceleration voltage was raised for forming a deep impurity range. As a p mold impurity, aluminum etc. may be used other than B.
[0036] a part of first mask which it left -- M1a is removed and N ion 4a is poured into the whole surface. [This drawing (f)]. 4b is poured-in N atom. This is for concentration control of the n channel field 50, acceleration voltage is 200keV(s) and a dose is abbreviation 1x1012cm-2. Before this, it is p+. Since the deep ion implantation for the embedding field 42 is performed, it is p+. B atom is poured into n drift layer 41b of the surface layer which comes on the embedding field 42. Resistance of a surface layer can be stabilized by impregnation of N ion. The high impurity concentration of the surface layer after heat treatment is abbreviation 5x1015cm-3. It becomes.
[0037] It is n+ by performing 1600 degrees C and heat treatment of 2 hours, and activating the poured-in impurity. The source field 43, p gate field 44, and p+ Each field of the embedding field 42 is formed [drawing 3 (a)]. Although diffusion of an impurity hardly breaks out in SiC as stated previously, the depth in which an impurity range is formed is controllable by accommodation of acceleration voltage. For example, p+ The embedding field 42 is made by the layer with a thickness of 0.5 micrometers at focusing on a depth of 0.8 micrometers by having made acceleration voltage high with 400keV(s), and n about 0.5-micrometer drift region 41b is left behind on it. p gate field 44 and n+ The depth of the source field 43 is about 0.2 micrometers.
[0038] To a front face, it is SiO2 by the CVD method. The film 2 is deposited [this drawing (b)]. It is n+ at RIE form the fourth mask M4 by the photolithography, and using the mixed gas of carbon tetrafluoride (CF4) and oxygen (O2). Crevice 47a which arrives at p+ embedding field 42 from the front face of the source field 43 is formed [this drawing (c)]. It is SiO2 at a photolithography. After forming opening for contact in the film 2 Pattern formation of the aluminium alloy film is vapor-deposited and carried out, and it considers as the source electrode 47 and the gate electrode 46., n+ A drain electrode is prepared also in the rear face of a substrate, and a process is completed [this drawing (d)].
[0039] By taking the above manufacture approaches, it was able to consider as the high proof-pressure SiC vertical mold JFET of drawing 1 . SiCJFET of an example 1 -- a part of first mask -- the edge of M1b -- n+ the source field 43 specifies -- having -- a part of first mask -- p gate field 44 is prescribed by another edge of M1b, and another partial M1a of the first mask. By partial M1a with the first still more nearly another mask, it is p+. The edge of the embedding field 42 is specified. Thus, since the impurity range is prescribed by only the first mask M1, each has consistency and the problem of the ununiformity by mask alignment, such as a location gap, cannot arise. After the pattern formation of the first mask M1, the advantage that the dimension of each impurity range can be checked is also.
[0040] Although the control is very important on application since the die length of a channel field is a main parameter which determines the property of MOSFET, in SiCJFET of this example 1, the n channel field 50 of the lower part of p gate field 44 serves as channel length substantially, channel length is formed with a precision short and sufficient to homogeneity, and the stable property and the high yield are obtained. The on resistance of JFET of 1500V class

made as an experiment showed 15m ohm-cm -2 and a low value.
[0041] Moreover, p+ The embedding field 42 was formed by the ion implantation with high acceleration voltage, the junction depth was written deeply, and high pressure-proofing beyond 1500V has been realized easily. By having been added like N ion grouting for high-impurity-concentration control to the surface layer of n drift layer 41b, the threshold voltage of MOSFET can be controlled and it can also be referred to as FET of no MARIOFU.
[0042] Some deformation is also considered as the manufacture approach. For example, n+ Reverse is sufficient as the sequence of the ion implantation for forming the source field 43 and p gate field 44. Moreover, the ion implantation for high-impurity-concentration control of the n channel field 50 may be performed first. If it will carry out at low temperature more instead of an elevated temperature which calls an ion implantation 1000 degrees C, the selection width of face of a mask ingredient can extend.
[0043] [Example 2] drawing 4 is the fragmentary sectional view of SiCJFET concerning the second example of this invention. This is the modification of the example 1 of drawing 1 . A crevice is not formed in a SiC substrate front face in this example, but it is p+ to the surface layer of n drift layer 51b. p+ which arrives at the embedding field 52 Contact field 52a is formed and it is n+ to that front face. The source field 53 and the common source electrode 57 are formed.
[0044] n+ As a mask (it is equivalent to M2 of drawing 2 (b)) in the case of N ion implantation for source field 53 formation, it is n+. The mask which also specifies the outside of the source field 53 is used, still more nearly another mask is used, and it is p+. What is necessary is just to perform B ion implantation for contact field 52a formation. If it does in this way, a crevice cannot be formed but an electrode can be prepared in a substrate front face.
[0045] n+ There is instead of [no] in a part of first mask (it being equivalent to M1b of drawing 2 (b)) specifying the inside of the source field 53, and the die length of a channel field is the same as that of SiCJFET of an example 1, the n channel field 60 of the lower part of p gate field 44 has short uniform channel length, it is form with a sufficient precision, and the stable property and the high yield are obtain.
[0046] [Example 3] drawing 5 is the fragmentary sectional view of SiCJFET concerning the third example of this invention. This can also say it also as deformation of SiCJFET of drawing 1 . The point different from SiCJFET of drawing 1 is a point that the gate electrode 66 touches common to p gate field 64 and the front face of n drift layer 61b. Here, the gate electrode 66 chooses a SiC substrate and a metal which forms the Schottky barrier, for example, Ti, aluminum, Pt, etc.
[0047] At JFET of an example 1, as for p gate field 44, contact is taken only in the part which the gate electrode 46 contacts so that drawing 1 may show. In order to stop this contact resistance small, the touch area had to be enlarged and the magnitude of this contact aperture had restricted the minimum value of the die length of a channel. Since JFET of this example 3 improves this point and the gate electrode 66 touches not only p gate field 64 but the front face of n drift layer 61b, a large contact part can be taken and it becomes possible to design a channel field narrowly.
[0048] It also sets to JFET of this example 3, and is n+. It is the same that the property which a source field carries out self align to the surface layer of p base region, and is formed, and channel length was formed with a uniformly and sufficient precision like JFET of an example 1, and was stabilized is acquired with the sufficient yield. However, the gate electrodes 66 are a SiC substrate and the metal which forms the Schottky barrier, and are not necessarily the same metal as the source electrode 67. Or the gate electrode 66 may be made into a bilayer with the same metal as the metal and the source electrode 67 which carry out Schottky contact. About the

process which manufactures this, it is almost almost the same as that of drawing 2 and 3, and explanation is omitted.
[0049] [Example 4] drawing 6 is the fragmentary sectional view of SiCMOSFET concerning the fourth example of this invention. n+ In the wafer with which the laminating of the n drift layer 71b was carried out by epitaxial growth on substrate 71a It is p+ from the front face of n drift layer 71b to a somewhat deep location. The embedding field 72 is formed and it is the p+. It is n+ to the surface layer of upper n drift layer 71b of the embedding field 72. Although the point that the source field 73 is formed is the same as an old example There is nothing and p gate field is p+. The upper part of the embedding field 72 is made into the n channel field 80, and the gate of metal-oxide-semiconductor structure is prepared on the front face.
[0050] That is, the gate electrode layer 76 which consists of a polycrystalline silicon layer through gate oxide 75 is formed on the front face of n drift layer 71b. 79 is an insulator layer of boron phosphorus silica glass (BPSG) which insulates the gate electrode layer 76 and the source electrode 77. n+ There is crevice 77a investigated from the front face of the source field 73, the front face is met, and it is n+. The source field 73 and p+ The source electrode 77 which contacts common to a front face with the embedding field 72 is formed, and it is n+. The rear face of substrate 71a is contacted and the drain electrode 78 is formed. The dimension of main each part is almost the same as the value stated in the example 1. The thickness of gate oxide 75 is [the thickness of 1 micrometer and an insulator layer 79 of the thickness of 50nm and the gate electrode layer 76] 2 micrometers.
[0051] When this MOSFET is also called ACCUFET and impresses a forward electrical potential difference to the gate electrode layer 76, induction of the accumulation layer is carried out to the surface part of n drift layer 71b of gate electrode layer 76 directly under, and a current flows between the drain electrode 78 and the source electrode 77. Moreover, if a negative electrical potential difference is impressed to the gate electrode layer 76, the current between the drain electrode 78 and the source electrode 77 can be intercepted, and it has a switching function. The electrical potential difference between source drains is p+. It is possible for it to be impressed between the embedding field 72 and n drift layer 71b, and to hold a big electrical potential difference, and it has structure suitable for high pressure-proofing.
[0052] Drawing 7 (a) thru/or (e) and drawing 8 (a) thru/or (d) are the fragmentary sectional views of the order of a production process near the front face of SiCMOSFET of the example 4 of drawing 6 . A process is explained in order of below. n+ 4 H-SiC substrate which carried out the laminating of the n drift layer 71b of a phosphorus dope with epitaxial growth is prepared on substrate 71a. The high impurity concentration of n drift layer 71b, thickness, etc. are the same as an example 1, and good. On the front face of the n drift layer 71b, a polycrystal silicone film is deposited with a reduced pressure CVD method, a pattern is formed by the photolithography, and it considers as the first mask M1 [drawing 7 (a)]. The first mask M1 consists of each part of M1a of a center section, and M1b of both sides. It is the same as that of an example 1 that it is not necessary to be necessarily a polycrystal silicone film of the first mask M1.
[0053] It is SiO2 by the heat CVD method on the first mask M1 of a polycrystal silicone film. After depositing the film, forming a pattern by the photolithography and considering as the second mask M2, the ion used as n mold impurity, for example, N ion 4a, is poured into the field specified with the second mask M1 and M2 for a start [these] [this drawing (b)]. This is n+. It is for source field 73 formation, and acceleration voltage, a dose, etc. are the same as an example 1, and good. this second mask M2 -- not necessarily -- SiO2 it is not necessary to be -- although -- since it is required to remove leaving the first mask M1 at a next process, unlike the first mask

M1, the ingredient which can perform alternative etching is chosen. Since the second mask M2 should just have an edge on the first mask M1, it is easy mask alignment. As an n mold impurity, P etc. is used other than N.

[0054] SiO2 the second membranous mask M2 -- removing -- a photolithography -- a part of first mask -- [this drawing (c)] which pours in the ion used as p mold impurity, for example, B ion 5a, after leaving M1a. This is p+. It is for embedding field 72 formation, and acceleration voltage is 400keV(s) and a dose is abbreviation 1x1015cm-2. Acceleration voltage was raised for forming a deep impurity range. As for p mold impurity, aluminum etc. is used other than B.

[0055] a part of first mask which it left -- M1a is removed and N ion 4a is poured in. [This drawing (d)]. This is for high-impurity-concentration control of the n channel field 80, acceleration voltage is 200keV(s) and a dose is abbreviation 1x1012cm-2. It is p+ by performing 1600 degrees C and heat treatment of 2 hours, and activating the poured-in impurity. The embedding field 72 and n+ Each field of the source field 73 and the n channel field 80 is formed [this drawing (e)].

[0056] SiO2 film which turns into gate oxide 75 by 1200 degrees C and thermal oxidation of 2 hours is formed in a front face, and about 1 micrometer of polycrystal silicone films 1 which serve as a gate electrode layer with a reduced pressure CVD method continuously is deposited [drawing 8 (a)]. It forms by thermal oxidation, and also gate oxide 75 can also form membranes by CVD. As an ingredient of the gate electrode layer 76, molybdenum (Mo) etc. is [other than polycrystalline silicon] usable.

[0057] A photoresist is applied, and after carrying out pattern formation of the polycrystal silicone film 1 by the photolithography and considering as the gate electrode layer 76, the insulator layers 79, such as boron phosphorus silica glass (BPSG), are deposited on a front face with a CVD method [this drawing (b)]. It is n+ at RIE form a pattern by the photolithography and using the mixed gas of carbon tetrafluoride (CF4) and oxygen (O2). The front face of the source field 73 to p+ Crevice 77a which arrives at the embedding field 72 is formed [this drawing (c)].

[0058] After forming opening for contact in an insulator layer 79 by the photolithography, pattern formation of the aluminium alloy is vapor-deposited and carried out, and it considers as the source electrode 77 and the gate electrode which is not illustrated. n+ A drain electrode is prepared also in the rear face of a substrate, and a process is completed [this drawing (d)]. MOSFET of this example 4 -- also setting -- a part of first mask -- the edge of M1b -- n+ The source field 73 is specified and the edge of p+ embedding field 72 is prescribed by partial M1a with the first another mask. Thus, since the impurity range is prescribed by only the first mask M1, each has consistency and the problem of the ununiformity by mask alignment, such as a location gap, cannot arise.

[0059] Therefore, like JFET of an example 1, about 1.5-micrometer channel length is realized with a uniformly and sufficient precision, and the stable property is acquired with the sufficient yield. After formation of the first mask 1, the advantage that the dimension of each impurity range can be checked is also. By being added like N ion grouting for high-impurity-concentration control to the surface layer of n drift layer 71b, and considering as the n channel field 80, the threshold voltage of MOSFET can be controlled and it can also be especially referred to as FET of no MARIOFU.

[0060] Moreover, since gate oxide 75 is formed on the SiC substrate at the plane, there is no problem of the stress of the electric field in the corner section of the gate oxide seen by MOSFET conventional trench type, and a raise in pressure-proofing is possible. Some deformation is also

considered as the manufacture approach. For example, the ion implantation for high-impurity-concentration control of the n channel field 80 may be performed first, and reverse order is sufficient as formation with the second mask M2 and the third mask M3.
[0061] n+ In the case of N ion implantation for source field 73 formation, it is n+. The mask which specifies the outside of the source field 73 is used, still more nearly another mask is used, and it is p+. If B ion implantation for contact field 52a formation is performed, crevice 77a cannot be formed but an electrode can be prepared in a substrate front face. In that case The die length of a channel field is formed in homogeneity with a sufficient precision like SiCMOSFET of an example 4, and the stable property and the high yield are obtained.
[0062] [Example 5] drawing 9 is the fragmentary sectional view of SiCMOSFET concerning the fifth example of this invention. n+ It is p+ to a somewhat deep location from the front face of n drift layer 81b deposited with epitaxial growth on substrate 81a. The embedding field 82 is formed and it is p+. The p base region 82 is formed in the surface layer of upper n drift layer 81b of the embedding field 82, and it is n+ alternatively in the upper part. The source field 83 is formed. And the part of the edge of the p base region 82 is n+. It is so characteristic that it keeps away from the source field 83 that the junction depth is shallow almost linearly. Moreover, it is p+ to a part deeper than the p base region 82 so that the p base region 82 may be overlapped in part. Contact field 82a is formed. n+ The upper part of the p base region 82 of a part in which the source field 83 is not formed is made into the n channel field 90, and the gate of the same metal-oxide-semiconductor structure as MOSFET of drawing 6 is prepared on it. That is, the gate electrode layer 86 which consists of a polycrystalline silicon layer through gate oxide 85 is formed. 89 is the insulator layer of BPSG which insulates a gate electrode layer and the source electrode 87. n+ From the front face of the source field 83, there is investigated crevice 87a and it is n+. The source field 83 and p+ It contacts common to a front face with the contact field 82, and the source electrode 87 is formed, and it is n+. The rear face of substrate 81a is contacted and the drain electrode 88 is formed.
[0063] Examples of the main dimensions are the following values. n+ For the high impurity concentration of substrate 41a, it of 1x1018cm in 350 micrometers in 3 and thickness and n drift layer 41b is 1x1016cm 10 micrometers in 3 and thickness. Spacing between 3 and a junction depth of 1.5 micrometers of 5x1016cm, and the p base region 82 of both sides of the highest high impurity concentration of the p base region 82 is about 6 micrometers. n+ The high impurity concentration of the source field 43 is 1x1019cm 3 and a junction depth of 0.2 micrometers, and width of face is about 5 micrometers and p+. The highest high impurity concentration of the contact field 82 is [the high impurity concentration of about 5 micrometers and the n channel field 90 of 3 and a junction depth of 2.0 micrometers of 1x1019cm, and width of face] 5x1015cm 3 and a junction depth of 0.5 micrometers. n+ Spacing between the edge of the source field 83 and the edge of the p base region 82 is about 2 micrometers. The depth of crevice 87a investigated from the front face is 0.7 micrometers, and width of face is about 3 micrometers. The pitch of the unit cell of drawing is about 30 micrometers. The thickness of gate oxide 85 is [the thickness of 1 micrometer and an insulator layer 89 of the thickness of 50nm and the gate electrode layer 86] 2 micrometers.
[0064] Drawing 10 (a) thru/or (e) and drawing 11 (a) thru/or (e) are the fragmentary sectional views of the order of a production process near the front face of SiCMOSFET of the example 5 of drawing 9 . A process is explained in order of below. First, n+ 4 H-SiC substrate which carried out the laminating of the n drift layer 81b of a phosphorus dope with epitaxial growth is prepared on a substrate. On the front face of n drift layer 81b, a polycrystal silicone film is

deposited with a reduced pressure CVD method, a pattern is formed by the photolithography, and it considers as the first mask M1.

[0065] It is important especially in the case of this patterning to form the taper section 8 in the edge of the first mask M1 over 1-2 micrometers. This is because channel length is controlled by the include angle of the taper section 8 of the first mask M1 in the ion implantation for the next p base region formation. Therefore, this cone angle must be captured and decided to be a predetermined design. And this include angle is controllable by choosing the etching conditions at the time of etching the thin film of the first mask 1 by plasma etching etc. Or a loose taper will be obtained, if an ion implantation is carried out to the upper part of a thin film, the damage is given to it and it carries out only near the front face that it is easy to be etched. There is also the approach of controlling a taper angle by controlling the dose of the ion implantation in that case.

[0066] The ion, for example, boron (B) ion 5a, which serves as p mold impurity by using the first mask M1 as a mask is poured in [drawing 10 (a)]. 5b is poured-in B atom. This is for p base region 82 formation, acceleration voltage is 300keV(s) and a dose is abbreviation 1x1015cm-2. Acceleration voltage was raised for forming a deep impurity range. In a field without the first mask M1, an impurity is poured in deeply, it becomes shallow almost linear gradually as thickness of the mask [first] M1 increases, and an impurity atom carries out distribution as shown in drawing. If thickness of the first mask M1 is made to some extent thin, an impurity impregnation field does not arrive at even a front face, but can be made into the field of an embedding mold. As for p mold impurity, aluminum etc. is used other than B. It is the same as that of an example 1 that it is not necessary to be necessarily a polycrystal silicone film of the first mask M1.

[0067] Next, the ion, for example, N ion 4a, which serves as n mold impurity by using the first same mask M1 as a mask is poured in [this drawing (b)]. 4b is poured-in n atom. This is for n+ source field 83 formation, and the 100keV(s) as an example 1 with the same acceleration voltage etc. and a dose are good at abbreviation 5x1015cm-2. In the field which does not have the first mask M1 in this case, either, an impurity is poured in deeply, if the first mask M1 becomes thick, it will become shallow gradually, and an impurity atom carries out distribution as shown in drawing. However, since acceleration voltage is made low, the field poured in differs from the impregnation field of B ion. If the include angle of the taper section 8 is the same, spacing of the impregnation field of p mold impurity and the impregnation field of n mold impurity will become fixed.

[0068] It is SiO2 by the heat CVD method on the first mask M1 of a polycrystal silicone film. The film 2 is deposited [this drawing (c)]. After forming a sidewall 9 in the side of ** and the taper section 8 of the first mask M1 carrying out overall etching by RIE, the ion used as p mold impurity, for example, B ion 5a, is poured into the field specified by these first masks M1 and the sidewall 9 [this drawing (d)]. This is high-concentration p+. It is for contact field 84 formation, and acceleration voltage, 400keV, and a dose are abbreviation 1x1015cm-2. As a p mold impurity, aluminum etc. is used other than B.

[0069] After removing the first mask M1 and a sidewall 9, N ion 4a is poured into the whole surface. [This drawing (e)]. This is for high-impurity-concentration control of the n channel field 90, acceleration voltage is 200keV(s) and a dose is abbreviation 1x1012cm-2. Thereby, a threshold is controllable. Each field is formed by performing 1600 degrees C and heat treatment of 2 hours, and activating the poured-in impurity [drawing 11 (a)]. Thus, p base region 82sn+ The source field 83 can be shifted and formed.

[0070] Heat SiO2 with a thickness of 50nm it is thin to gate oxide 85 on a front face with 1200

degrees C and thermal oxidation of 2 hours The film 6 is formed, and about 1 micrometer of polycrystal silicone films 1 is continuously deposited with a reduced pressure CVD method [this drawing (b)]. It forms by thermal oxidation, and also gate oxide 85 can also form membranes by CVD. After applying a photoresist, carrying out pattern formation of the polycrystal silicone film 1 by the photolithography and considering as the gate electrode layer 86, with a CVD method, the insulator layers 89, such as boron phosphorus silica glass (BPSG), are deposited on a front face, and a pattern is formed in it by the photolithography [this drawing (c)].

[0071] At RIE using the mixed gas of carbon tetrafluoride (CF4) and oxygen (O2), it is p+ from the front face of n+ source field 83. Crevice 87a which reaches contact field 82a is formed [this drawing (d)]. After forming opening for contact in an insulator layer 89 by the photolithography, pattern formation of the aluminium alloy is vapor-deposited and carried out, and it considers as the source electrode 87 and the gate electrode which is not illustrated [this drawing (e)]. n+ A drain electrode is prepared also in the rear face of a substrate, and a process is completed.

[0072] In MOSFET of this example 5, the edge of n+ source field 83 and the p base region 82 is prescribed by by making the edge of the first mask 1 into the shape of a taper, and changing the acceleration voltage in the case of impregnation of p mold impurity and n mold impurity. That is, the channel length who is spacing between both is prescribed by the taper section 8 of the first mask M1. Thus, since the impurity range is prescribed by only the first mask, both have consistency and the problem of the ununiformity by mask alignment, such as a location gap, does not occur.

[0073] Therefore, channel length is formed in homogeneity with a sufficient precision, and the stable property is acquired with the sufficient yield. Moreover, if the include angle of the taper section 8 of the first mask M1 is changed, both spacing, i.e., the die length of a channel field, can be controlled freely, and the balance of on resistance and pressure-proofing will also tend to take it. After formation of the first mask 1, the advantage that the dimension of each impurity range can be checked is also.

[0074] By having been added like N ion grouting for high-impurity-concentration control to the surface layer of n drift layer 81b, the threshold voltage of MOSFET can be controlled and it can also be especially referred to as FET of no MARIOFU. Some deformation is also considered as the manufacture approach. For example, the ion implantation for high-impurity-concentration control of the n channel field 90 may be performed first. Moreover, impregnation and n+ of B ion for the p base region 82 Reverse is sufficient as the order of impregnation of N ion for source field 83 formation. A sidewall field is formed first and it is p+. The ion implantation for contact field 84 formation may be performed.

[0075] Since gate oxide 85 is formed on the SiC substrate also in this example at the plane, there is no problem of the stress of the electric field in the gate oxide corner section seen by MOSFET conventional trench type, and a raise in pressure-proofing is possible. Moreover, at this example, it is p+. It is n+, although contact field 82a was embedded and being considered as the field of a mold. In the case of N ion implantation for source field 83 formation, it is n+. The mask which specifies the outside of the source field 83 is used, and it is p+. If contact field 82a is made to arrive at even a front face by multiplex impregnation, the source electrode 87 can be formed in a substrate front face, and there will be no need of forming crevice 87a.

[0076] [Example 6] drawing 12 (a) thru/or (e) are the fragmentary sectional views near the front face of the order of a production process for explaining the another manufacture approach of the almost same SiCMOSFET as SiCMOSFET of drawing 9 . A process is explained in order of below. First, n+ 4 H-SiC substrate which carried out the laminating of the n drift layer 91b of a

phosphorus dope with epitaxial growth is prepared on a substrate. The high impurity concentration of n drift layer 91b, thickness, etc. are the same as an example 1, and good. On the front face of the n drift layer 91b, it is SiO2 with a thickness of about 2 micrometers by the plasma-CVD method. The film 2 is deposited, a pattern is formed by the photolithography, and it considers as the third mask M3.

[0077] The ion, for example, B ion 5a, which serves as p mold impurity by using the third mask M3 as a mask is poured in [drawing 12 (a)]. 5b is poured-in B atom. This is high-concentration p+. It is for contact field 94 formation, and acceleration voltage, 400keV, and a dose are abbreviation 1x1015cm-2. As a p mold impurity, aluminum etc. is used other than B.

[0078] Next, CF4+H2 It considers as the first mask M1 which carried out etchback of the third mask M3, and made the edge the shape of a taper over 1-2 micrometers by plasma etching using gas [this drawing (b)]. At this time, the whole thickness also becomes thin and thickness is set to about 1 micrometer. In the ion implantation for the next p base region formation, a channel is controlled by the cone angle of the edge of the first mask by this like the time of SiCMOSFET of an example 5.

[0079] The ion, for example, B ion 5a, which serves as p mold impurity by using as a mask the first mask M1 which made the edge the shape of a taper is poured in [this drawing (c)]. This is for p base region 92 formation, acceleration voltage is 300keV(s) and a dose is abbreviation 1x1015cm-2. In a field without the first mask M1, an impurity is poured in deeply, it becomes shallow gradually as thickness of the mask [first] M1 increases, and an impurity atom carries out distribution as shown in drawing.

[0080] Next, the ion, for example, N ion 4a, which serves as n mold impurity by using as a mask the first mask M1 which made the same edge the shape of a taper is poured in [this drawing (d)]. This is n+. It is for source field 93 formation, and acceleration voltage is 100keV(s) and a dose is abbreviation 5x1015cm-2. Since acceleration voltage is made low, the field poured in differs from the impregnation field of p mold impurity.

[0081] After removing the first mask M1, N ion 4a is poured into the whole surface. [This drawing (e)]. This is for high-impurity-concentration control of the n channel field of the surface layer of n drift layer 91b, acceleration voltage is 200keV(s) and a dose is abbreviation 1x1012cm-2. Thereby, a threshold is controllable. After this, activation of the impurity poured in after drawing 10 (a), formation of an electrode, etc. are performed.

[0082] Since back dirty [of the third mask M3] was carried out and it considered as the first mask M1 when taking this approach, it is not necessary to form a mask ingredient anew. And since the include angle of the taper section also becomes homogeneity and spacing of the p base region 92 and n source field 93 is specified, both have consistency and the problem of the ununiformity by mask alignment, such as a location gap, cannot arise. And channel length is formed in homogeneity with a sufficient precision, and the stable property is acquired with the sufficient yield.

[0083] Some deformation is also considered as the manufacture approach. For example, a reverse order is sufficient as impregnation [drawing 12 (c)] of p mold impurity ion for p base region formation, and impregnation [drawing 12 (d)] of n mold impurity ion for n source field formation, and the ion implantation for high-impurity-concentration control of an n channel field [drawing 12 (e)] may be performed first.

[0084]

[Effect of the Invention] As explained above, according to this invention, it sets to the manufacture approach of silicon carbide vertical FET. Some of one [of the first mask] edges

prescribe the first conductivity-type impurity installation field using the first mask and the second mask which overlaps in part. By removing the first some masks and second mask, and specifying the second conductivity-type impurity installation field by another part of the first mask, the first conductivity-type impurity installation field and the second conductivity-type impurity installation field are formed in self align.

[0085] If the approach of changing and carrying out the ion implantation of the acceleration voltage is taken using the mask which made especially the edge the shape of a taper, the first conductivity-type impurity installation field and the second conductivity-type impurity installation field can be formed in self align only with one mask. By controlling the high impurity concentration of a channel field, threshold voltage can be controlled and it can be referred to as FET of no MARIOFU.

[0086] Thus, JFET and MOSFET with the former very difficult very precise channel field can be realized now, and effectiveness was brought to reduction of on resistance. This invention is an approach very effective not only in FET according to individual but CMOS-IC and other SiC semiconductor devices, and makes easy manufacture of the silicon carbide semiconductor device of high pressure-proofing.

[Translation done.]

TECHNICAL FIELD

[Field of the Invention] This invention relates to the manufacture approach of a vertical mold field-effect transistor (it is described as Following FET) and the vertical mold electric field effect FET with the gate of the assembling die which used silicon carbide as a semiconductor material and which is a power semiconductor device, or the MOS mold of metal-oxide film-semi-conductor structure.

[Translation done.]

PRIOR ART

[Description of the Prior Art] Since a band gap is large and the maximum insulation electric field are large a figure single [about] as compared with silicon (it is described as Following Si), silicon carbide (it is described as Following SiC) is an ingredient with which the application to a next-generation power semiconductor device is expected. It is applied to various electron devices until now using the single crystal wafer called 4 H-SiC or 6 H-SiC, and it is thought that it is especially suitable for an elevated temperature and the component for large power. The above-mentioned crystal is the alpha phase SiC of the form which carried out the laminating of a sphalerite mold and the wurtzite mold. The semiconductor device is made also for the crystal of the beta phase SiC otherwise called 3 C-SiC as an experiment. [, for example, Weitzel, by which CMOS-IC which is the general-purpose semiconductor devices, such as schottky diode, end-fire array MOSFET, and a thyristor, as a component for power is recently made as an experiment, and it is checked from the property as compared with the conventional Si semiconductor device that a property is very good, :IEEE Trans.on Electron Devices besides C.W., and vol. -- 43, No.10, and pp.1732-1741 --] (1997) . Some examples of MOSFET are shown below.
[0003] Drawing 13 is the fragmentary sectional view of the unit cell of junction type FET (it omits Following JFET) currently developed as one of the RF components [and Abstracta of Int.Conf.on Silicon Carbide besides Sheppard and S.T., III-Nitrides and Related Materials] (1997). p+ It is n+ to the surface layer of n drift layer 11 by which the laminating was carried out on the substrate 10. The source field 13, p gate field 15, and n+ The drain field is formed. n+ The source field 13 and n+ The drain field 14 and p gate field 15 are contacted, and the source electrode 17, the drain electrode 18, and the gate electrode 16 are formed, respectively.
[0004] When an electrical potential difference is impressed to the gate electrode 16 with this structure, they are p gate field 15 to p gate field 15, and p+. A depletion layer spreads to the n channel field 20 between substrates 10. The current between the source electrode 17 and the drain electrode 18 is controlled by this. Moreover, a current flows again between the drain electrode 18 and the source electrode 17 by removing the electrical potential difference impressed to the gate electrode 16. Thus, the current between source drains serves as a component switchable [with gate voltage]. Since this JFET depletion-izes a channel field by electrical-potential-difference impression to the gate electrode 16, it is called a depletion type. A front face to p+ The slot which reaches a substrate 10 is formed and it fills up with the insulator layer 19 because [of isolation].
[0005] On the other hand, drawing 14 is one sort of a vertical mold MOSFET [Shenoy, J.N. others , Abstracta of Int.Conf.on Silicon Carbide, III-Nitrides and Related Materials] (1997). n+ It is p+ by the ion implantation of high acceleration voltage [surface layer / of n drift layer 21b by which the laminating was carried out on substrate 21a]. The embedding field 22 is formed. The p+ It is n+ to the surface layer of n drift layer part 21b on the embedding field 22. The

source field 23 is formed. Two n+ The gate electrode 26 is formed through gate dielectric film 25 on the front face of n drift layer part 21b inserted into the source field 23. n+ The source electrode 27 is n+ to the front face of the source field 23. The drain electrode 28 is formed in the rear face of substrate 21a, respectively.

[0006] In this example, the gate part has metal-oxide-semiconductor structure which impresses an electrical potential difference through gate dielectric film 25 instead of pn junction. In this MOSFET, by impressing a forward electrical potential difference to the gate electrode layer 26, induction of the accumulation layer is carried out to the n channel field 30 of the surface part of n drift layer 21b of gate electrode 26 directly under, and a current flows between the drain electrode 28 and the source electrode 27. Moreover, if a negative electrical potential difference is impressed to the gate electrode 26, the current between the drain electrode 28 and the source electrode 27 can be intercepted, and it has a switching function. The electrical potential difference between source drains is p+. It is possible for it to be impressed between the embedding field 22 and n drift layer 21b, and to hold a big electrical potential difference, and it is made the structure suitable for high pressure-proofing. Since this MOSFET forms an accumulation layer by electrical-potential-difference impression to the gate electrode 26, it is called ACCUFET.

[0007] Drawing 15 is [and Phys.Stat.Sol. (a) besides Onda and S., vol.162, and p.369] (1997) which are the fragmentary sectional view of the unit cell of another vertical mold quantity proof-pressure MOSFET **. . n+ The p base region 32 is formed on substrate 31a at the surface layer of n drift layer 31b by which the laminating was carried out, and it is n+ to the surface layer of the p base region 32. The source field 33 is formed. Two n+ The n channel field 40 which connects the source field 33 is formed of epitaxial growth, and the gate electrode layer 36 is formed through gate dielectric film 35 on the front face of the n channel field 40. n+ The source electrode 27 is n+ to the front face of the source field 33. The drain electrode 38 is formed in the rear face of substrate 31a, respectively.

[0008] By impressing a forward electrical potential difference to the gate electrode layer 36 also in this case, induction of the accumulation layer is carried out to the surface part of the n channel field 40 of gate electrode layer 36 directly under, and it becomes possible to pass the current from the drain electrode 38 to the source electrode 37. Moreover, between the drain electrode 38 and the source electrodes 27 will be intercepted, and by impressing a negative electrical potential difference to the gate electrode layer 36 will show a switching function.

[0009] Otherwise, although there is also an example of a prototype of MOSFET of a planar mold or a trench mold, by SiC, that the mobility of an inversion layer is very small gets down that it is experimentally sudden, and it is thought that FET of the enhancement type using an inversion layer is not suitable for practical use. It is the example of the structure where have the common description in that it is not FET of the enhancement type with which the component of the three above-mentioned examples uses an inversion layer to it but FET using the semi-conductor layer of a conductivity type from the first as a channel, especially it is suitable for SiC.

[Translation done.]

EFFECT OF THE INVENTION

[Effect of the Invention] As explained above, according to this invention, it sets to the manufacture approach of silicon carbide vertical FET. Some of one [of the first mask] edges prescribe the first conductivity-type impurity installation field using the first mask and the second mask which overlaps in part. By removing the first some masks and second mask, and specifying the second conductivity-type impurity installation field by another part of the first mask, the first conductivity-type impurity installation field and the second conductivity-type impurity installation field are formed in self align.

[0085] If the approach of changing and carrying out the ion implantation of the acceleration voltage is taken using the mask which made especially the edge the shape of a taper, the first conductivity-type impurity installation field and the second conductivity-type impurity installation field can be formed in self align only with one mask. By controlling the high impurity concentration of a channel field, threshold voltage can be controlled and it can be referred to as FET of no MARIOFU.

[0086] Thus, JFET and MOSFET with the former very difficult very precise channel field can be realized now, and effectiveness was brought to reduction of on resistance. This invention is an approach very effective not only in FET according to individual but CMOS-IC and other SiC semiconductor devices, and makes easy manufacture of the silicon carbide semiconductor device of high pressure-proofing.

[Translation done.]

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] When it is going to manufacture the semiconductor device for power, the actual former not much good property is not realized, or the structure of drawing 13 , and 14 or drawing 15 is not manufactured in fact, although the property which was very excellent is expected. It is the double diffusion MOS (D-MOS) whose one of the reason of the is an approach which has spread most with Si semi-conductor. Structure is in an easily unrealizable point in SiC. In Si, a precise channel consistency is realized by introducing p mold impurity and n mold impurity alternatively with the same mask, and carrying out thermal diffusion. Namely, the dimension of the.channel which influences the property of MOSFET is very controllable to a precision, and can make MOSFET with the sufficient yield.
[0011] It receives that can come and it is alike, and by SiC, the rate of activation of the impurity which carried out the ion implantation is bad, in order to raise this, an ion implantation 1000 degrees C or more and heat-of-activation processing at 1600 degrees C or more are required, and the diffusion of an impurity which carried out the ion implantation hardly breaks out. Therefore, installation of p mold impurity and n mold impurity must be depended on a respectively separate mask, and control of a precise channel consistency is not realized. Therefore, it becomes the thing also with the very big variation which has large channel resistance, and resistance of the whole component is like [as which it will be mostly specified by channel resistance]. It can be said that the property of SiC original is not acquired.
[0012] In view of the above problem, the purpose of this invention can realize a very precise channel, and is to offer the manufacture approach of silicon carbide vertical FET and silicon carbide vertical FET which can be high-pressure=proofed easily.

[Translation done.]

MEANS

[Means for Solving the Problem] The first conductivity-type drift layer which this invention becomes from the silicon carbide by which the laminating was carried out on the first conductivity-type silicon carbide substrate for the above-mentioned technical-problem solution, The second conductivity-type gate field and the first conductivity-type source field which isolated to the surface layer of the first conductivity-type drift layer mutually alternatively, and were formed in it, The second conductivity-type embedding field alternatively formed in the lower part of the second conductivity-type gate field and the first conductivity-type source field, The gate electrode layer contacted and prepared in the front face of the second conductivity-type gate field, In the manufacture approach of the end-fire array FET which has the source electrode which contacted the front face of the first conductivity-type source field and the second conductivity-type embedding field in common, and was prepared in it, and the drain electrode prepared in the rear face of a silicon carbide substrate some of one [of the first mask] edges -- one edge of the first conductivity-type source field -- specifying -- some other ends of the first mask, and other parts of the first mask -- the second conductivity-type gate field -- ** -- probably -- ** -- Other parts of said first mask shall prescribe the edge of the second conductivity-type embedding field.

[0014] For example, the substrate with which the laminating of the first conductivity-type drift layer which consists of silicon carbide on the first conductivity-type silicon carbide substrate was carried out by epitaxial growth as a concrete process is used. The process which forms the first mask on the front face of the first conductivity-type drift layer, The process which forms the second mask which consists of an ingredient which is different from the first mask so that the first mask and part may overlap, The process which introduces the impurity for the first conductivity-type source field formation into the surface layer of the first conductivity-type drift layer alternatively with those masks, The process which forms the third mask which consists of a process which removes the second mask, and an ingredient which is different from the first mask so that the first mask and part may overlap, The process which introduces the impurity for the second conductivity-type gate field formation into the surface layer of the first conductivity-type drift layer alternatively with those masks, The process which leaves a part of first mask and removes the first mask and the third mask, The process which introduces the impurity for the second conductivity-type embedding field formation into the surface layer of the first conductivity-type drift layer alternatively with the mask, The heat treatment process for activating the introduced impurity, and the process which forms the fourth mask in a silicon carbide substrate front face, The process which forms the crevice which arrives at the second conductivity-type embedding field from the front face of the first conductivity-type source field with the mask, It shall consist of the process which forms the fifth mask which consists of an insulating material, a process which vapor-deposits a metal membrane, and a process which

forms the gate electrode which consists of the metal membrane, a source electrode, and a drain electrode.
[0015] If it is made such, since the substantial dimension of a channel field is decided in the second conductivity-type gate field, the ununiformity by mask alignment will be avoided and precise control will be attained. It is possible for this to manufacture small FET of on resistance. Instead of forming the crevice which arrives at the second conductivity-type embedding field from the front face of the first conductivity-type source field, and preparing a source electrode, the second conductivity-type contact field which arrives at the second conductivity-type embedding field may be formed. If it is made such, a source electrode can be prepared on a front face.
[0016] Also in the thing to which each installation of the impurity for the first conductivity-type source field, the second conductivity-type gate field, and the second conductivity-type embedding field formation is especially performed by the ion implantation, then SiC, formation of an impurity range can be performed certainly. The electrode which forms the front face and the Schottky barrier of the first conductivity-type drift layer may be prepared.
[0017] If it is made such, it can consider as a channel field smaller than the dimension of the second conductivity-type gate field required for contact resistance. Moreover, the first conductivity-type drift layer which consists of silicon carbide by which the laminating was carried out on the first conductivity-type silicon carbide substrate, The first conductivity-type source field alternatively formed in the surface layer of the first conductivity-type drift layer, The second conductivity-type embedding field alternatively formed in the lower part of the first conductivity-type source field, The gate electrode layer prepared through gate dielectric film on the front face of the first conductivity-type drift layer, In the manufacture approach of the end-fire array FET which has the source electrode which contacted the front face of the first conductivity-type source field and the second conductivity-type embedding field in common, and was prepared in it, and the drain electrode prepared in the rear face of a silicon carbide substrate One edge of the first conductivity-type source field shall be specified with a part of first mask, and other parts of said first mask shall prescribe the edge of the second conductivity-type embedding field.
[0018] For example, the substrate with which the laminating of the first conductivity-type drift layer which consists of silicon carbide on the first conductivity-type silicon carbide substrate was carried out by epitaxial growth as a concrete process is used. The process which forms the first mask on the front face of the first conductivity-type drift layer, The process which forms the second mask which consists of an ingredient which is different from the first mask so that the first mask and part may overlap, The process which introduces the impurity for the first conductivity-type source field formation into the surface layer of the first conductivity-type drift layer alternatively with those masks, The process which leaves a part of first mask and removes the first mask and the second mask, The process which introduces the impurity for the second conductivity-type embedding field formation into the surface layer of the first conductivity-type drift layer alternatively with those masks, The process which removes a part of first mask which it left, and the heat treatment process for activating the introduced impurity, The process which forms gate oxide in a silicon carbide substrate front face by thermal oxidation, The process which carries out pattern formation after depositing a polycrystalline silicon layer on the gate oxide, The process which forms the third mask after covering an insulator layer, and the process which forms the crevice which arrives at the second conductivity-type embedding field from the front face of the first conductivity-type source field with the mask, It shall consist of a process

which prepares the aperture for contact in an insulator layer, and vapor-deposits a metal membrane, and a process which forms the gate electrode which consists of the metal membrane, a source electrode, and a drain electrode.

[0019] Since the dimension of a channel field is decided with the first mask also in this case, the ununiformity by mask alignment is avoided and precise control is attained. Instead of forming the crevice which arrives at the second conductivity-type embedding field from the front face of the first conductivity-type source field, and preparing a source electrode, the second conductivity-type contact field which arrives at the second conductivity-type embedding field may be formed. If it is made such, a source electrode can be prepared on a front face.

[0020] A part with the thickness of the first mask of the shape of a taper with a loose edge thick as an option can prescribe one edge of the first conductivity-type source field, and a part with the thin thickness of the first mask of said first mask can also prescribe the edge of the second conductivity-type base region. For example, the substrate with which the laminating of the first conductivity-type drift layer which consists of silicon carbide on the first conductivity-type silicon carbide substrate was carried out by epitaxial growth as a concrete process is used. The process which forms the first mask on the front face of the first conductivity-type drift layer, The process which forms the first mask of the shape of a taper with a loose edge, and the process which introduces the impurity for the first conductivity-type source field formation into the surface layer of the first conductivity-type drift layer alternatively by the part with the thick thickness of the mask, The process which introduces the impurity for the second conductivity-type base region formation into the surface layer of the first conductivity-type drift layer alternatively by the part with the thick thickness of the first mask, The process which forms the third mask in a silicon carbide substrate front face, and the process which introduces the impurity for the second conductivity-type contact field formation which arrives at the second conductivity-type base region with the mask, The process which removes the first mask, and the heat treatment process for activating the introduced impurity, The process which forms gate oxide in a silicon carbide substrate front face by thermal oxidation, It shall consist of the process which carries out pattern formation after depositing a polycrystalline silicon layer on the gate oxide, the process which covers an insulator layer, a process which prepares the aperture for contact in an insulator layer, and vapor-deposits a metal membrane, and a process which forms the gate electrode which consists of the metal membrane, a source electrode, and a drain electrode.

[0021] Since the dimension of a channel field is decided with the first mask also in this case, the ununiformity by mask alignment is avoided and precise control is attained. And another mask for impurity range formation is not needed. The crevice which arrives at the second conductivity-type base region from the front face of the first conductivity-type source field may be formed, and the source electrode in contact with the first conductivity-type source field and the second conductivity-type contact field may be prepared.

[0022] It is good to add the impurity installation process for the second conductivity-type contact field formation by using as a mask the process which prepares a sidewall in the side of the first mask especially, and the first mask and sidewall. If it is made such, it will not be based on mask alignment but formation of the second conductivity-type base region and the shifted second conductivity-type contact field can be performed.

[0023] The third mask with the thick thickness for the second conductivity-type contact field formation is formed, after passing through the process which introduces an impurity with the mask previously, etchback of the third mask can be carried out, and an edge can consider as the

first mask of the shape of a loose taper. If it is made such, the first mask and third mask of a basis will be the same, and will not have the need of forming another mask ingredient.
[0024] Furthermore, also in the thing to which each installation of the impurity for the first conductivity-type source field, the second conductivity-type embedding field, and the second conductivity-type base region formation is performed by the ion implantation, then SiC, formation of an impurity range can be performed certainly. And the process which introduces the first conductivity-type impurity for high-impurity-concentration control of a channel field into the whole surface of the surface layer of the first conductivity-type drift layer shall be added.
[0025] By controlling the high impurity concentration of a channel field, threshold voltage can be controlled and it can be referred to as FET of no MARIOFU. The first conductivity-type drift layer which consists of silicon carbide by which the laminating was carried out on the first conductivity-type silicon carbide substrate by the above manufacture approaches, The second conductivity-type base region where at least the part was alternatively embedded and formed in the surface layer of the first conductivity-type drift layer, The first conductivity-type source field formed in a part of upper part of the second conductivity-type base region in contact with the second conductivity-type base region, The gate electrode layer prepared through gate dielectric film on the channel field which is the first conductivity-type drift layer left behind on the second conductivity-type base region, The source electrode which contacted the front face of the first conductivity-type source field and the second conductivity-type base region in common, and was prepared in it, If it considers as the silicon carbide end-fire array FET which becomes shallow almost linearly so that it has the drain electrode prepared in the rear face of a silicon carbide substrate and the junction depth of the edge of the second conductivity-type base region keeps away from the first conductivity-type source field Control of the die length of a channel field is easy, and the end-fire array FET with a uniform channel field can manufacture easily.
[0026] From the second conductivity-type base region, even if it prepares the second conductivity-type contact field where the junction depth is deeper than the second conductivity-type base region and contacts a source electrode on the front face of the second conductivity-type contact field with high high impurity concentration, the crevice which arrives at the second conductivity-type contact field from the front face of the first conductivity-type source field is prepared, and a source electrode may be contacted on the exposure front face of the second conductivity-type contact field, so that a part may overlap the second conductivity-type base region.
[0027] If there is no need of preparing a crevice if a source electrode is contacted on the front face of the second conductivity-type contact field on the same front face as the first conductivity-type source field, the crevice which arrives at the second conductivity-type contact field from the front face of the first conductivity-type source field is prepared and a source electrode is contacted, there will be no need of thickening thickness of the second conductivity-type contact field. By controlling the thing which is high concentration, then high impurity concentration from that of the first conductivity-type drift layer, the high impurity concentration of a channel field can control threshold voltage, and can set to FET of no MARIOFU.
[0028]
[Embodiment of the Invention] Below, this invention is explained to a detail, while an example is shown. However, explanation is omitted about drawing 13 -15, a common part, or a part without this invention or instead of. Although n channel MOS FET is taken for the example as an important application of this invention, of course, this invention can be adapted also for p channel MOS FET which made the conductivity type reverse. In addition, the silicon carbide

explained here is aimed at what is mainly called 6H and 4H, although many polytypes exist as known well.

[0029] [Example 1] drawing 1 is the first example (it is described as an example 1 below.) of this invention. the following -- being the same -- it is the sectional view of the unit cell of starting SiCJFET. This supports the component which formed the conventional component of drawing 13 into high pressure-proofing. n+ It sets to the wafer with which the laminating of the n drift layer 41b was carried out by epitaxial growth on substrate 41a, and is p+ from the front face of n drift layer 41b to a somewhat deep location. The embedding field 42 is formed and it is p+. In the surface layer of upper n drift layer 41b of the embedding field 42, they are p gate field 44 and n+. The source field 43 is formed. The gate electrode 46 is formed on the front face of p gate field 44. n+ From the front face of the source field 43, the front face of investigated crevice 47a is met, and it is n+. The source field 43 and p+ It contacts common to a front face with the embedding field 42, and the source electrode 47 is formed, and it is n+. The rear face of substrate 41a is contacted and the drain electrode 48 is formed.

[0030] Examples of the main dimensions are the following values. n+ For the high impurity concentration of substrate 41a, it of 1x1018cm in 350 micrometers in 3 and thickness and n drift layer 41b is 1x1016cm 10 micrometers in 3 and thickness. p+ The highest high impurity concentration of the embedding field 42 is 5x1018cm 0.5 micrometers in 3 and thickness, and n 0.5-micrometer drift layer 41b is on it. p+ of both sides Spacing between the embedding fields 42 is about 5 micrometers. n+ The high impurity concentration of the source field 43 is 1x1019cm 3 and a junction depth of 0.2 micrometers, and width of face is [3 and a junction depth of 0.2 micrometers of 5x1018cm, and the width of face of it of about 3 micrometers and p gate field 44] about 2 micrometers. n+ Spacing between the source field 43 and p gate field 44 is about 1 micrometer, and n drift layer 41b has arrived at the front face. The depth of crevice 47a investigated from the front face is 0.7 micrometers, and width of face is about 3 micrometers. The pitch of the unit cell of drawing is about 25 micrometers.

[0031] Although the point different from the horizontal type JFET of drawing 13 is a point that the source electrode 47 and the drain electrode 48 serve as FET of the vertical mold formed in both sides of a semi-conductor substrate, the actuation is not fundamentally different from the thing of drawing 11 . That is, a depletion layer is breadth and n+ by impressing an electrical potential difference to the gate electrode 46 to the channel field 50 of p gate field 44 to a lower part. The source field 43 and n drift layer 41b are insulated electrically. As a result, the current from the drain electrode 38 to the source electrode 37 is controlled. It is JFET same depression type as what was shown in drawing 13 .

[0032] Drawing 2 (a) thru/or (f) and drawing 3 (a) thru/or (d) are the fragmentary sectional views near the front face of the order of a production process for explaining the manufacture approach of SiCJFET of the example 1 of drawing 1 . It explains in order of below. First, n+ 4 H-SiC substrate which carried out the laminating of the n drift layer 41b of a phosphorus dope with epitaxial growth is prepared on substrate 41a. For example, the high impurity concentration of n drift layer 41b is 1x1016cm-3, and thickness is 10 micrometers. On the front face of the n drift layer 41b, the polycrystal silicone film 1 is deposited with a reduced pressure CVD method, a pattern is formed by the photolithography, and it considers as the first mask M1 [drawing 2 (a)]. The first mask M1 consists of each part of M1a of a center section, and M1b of both sides. Thickness of the polycrystal silicone film 1 was set to 1 micrometer. The first mask M1 does not necessarily need to be a polycrystal silicone film, and as long as it turns into a mask of alternative etching, it may be the oxidization silicon film (henceforth, SiO2 it is described as the

film) well used for a silicon process etc., the nitriding silicon film, or a photoresist. However, to carry out an ion implantation at an elevated temperature, it is necessary to use the ingredient which ceases to the elevated temperature of polycrystalline silicon etc.
[0033] It is SiO2 by the heat CVD method on the first mask M1 of the polycrystal silicone film 1. After depositing the film 2, forming a pattern by the photolithography and considering as the second mask M2, the ion used as n mold impurity, for example, nitrogen (it is described as Following N) ion 4a, is poured into the field specified with the second mask M1 and M2 for a start [these] [this drawing (b)]. 4b is poured-in N atom. This is n+. It is for source field 43 formation, and acceleration voltage is 100keV(s) and a dose is abbreviation 5x1015cm-2. The temperature at the time of an ion implantation is about 800 degrees C. The rate of activation can be raised by carrying out an ion implantation at an elevated temperature. The second mask M2 is not necessarily SiO2. Although it is not necessary to be the film, since it is required to remove leaving the first mask M1 at a next process, it considers as a different ingredient from the first mask M1, and it can be necessary to be made to perform alternative etching. For example, when a polycrystal silicone film is used as the first mask M1, it is SiO2 like the upper example as the second mask M2. If the film is used, only the second mask 2 is removable with fluoric acid. It is SiO2 by reactive ion etching (it is described as Following RIE) the reverse is also possible and using the mixed gas of a carbon tetrachloride and oxygen etc. in that case. It is possible to control the etch rate of the film and a polycrystal silicone film, and to etch only a polycrystal silicone film. Thus, alternative removal is just performed to the first mask M1. Since the second mask M2 should just have an edge on the first mask M1, it is easy mask alignment. As an n mold impurity, phosphorus (it is described as Following P) etc. is used other than N.
[0034] SiO2 The second membranous mask M2 is removed and it is SiO2 by the heat CVD method again. After depositing the film 2, forming a pattern by the photolithography and considering as the third mask M3, the ion used as p mold impurity, for example, boron (it is described as Following B) ion 5a, is poured into the field specified with the third mask M1 and M3 for a start [these] [this drawing (c)]. 5b is poured-in B atom. This is for p gate field 44 formation, acceleration voltage is 100keV(s) and a dose is abbreviation 5x1015cm-2. Also in this case, the third mask M3 is not necessarily SiO2. It is not necessary to be the film and alternative removal is just performed to the first mask M1 at a next process. Since the third mask M3 should just have an edge on the first mask M1, it is easy mask alignment. As p mold impurity and a becoming impurity, aluminum (it is described as Following aluminum) etc. can be used other than B.
[0035] SiO2 the third membranous mask M3 -- removing -- a photolithography -- ** -- a part of first mask -- M1b -- removing -- a part of first mask -- [this drawing (d)] which leaves M1a. a part of first mask which it left -- M1a is used as a mask and B ion 5a is poured in again. [This drawing (e)]. This is p+. It is for embedding field 42 formation, and acceleration voltage is 400keV(s) and a dose is abbreviation 1x1015cm-2. Acceleration voltage was raised for forming a deep impurity range. As a p mold impurity, aluminum etc. may be used other than B.
[0036] a part of first mask which it left -- M1a is removed and N ion 4a is poured into the whole surface. [This drawing (f)]. 4b is poured-in N atom. This is for concentration control of the n channel field 50, acceleration voltage is 200keV(s) and a dose is abbreviation 1x1012cm-2. Before this, it is p+. Since the deep ion implantation for the embedding field 42 is performed, it is p+. B atom is poured into n drift layer 41b of the surface layer which comes on the embedding field 42. Resistance of a surface layer can be stabilized by impregnation of N ion. The high impurity concentration of the surface layer after heat treatment is abbreviation 5x1015cm-3. It

becomes.
[0037] It is n+ by performing 1600 degrees C and heat treatment of 2 hours, and activating the poured-in impurity. The source field 43, p gate field 44, and p+ Each field of the embedding field 42 is formed [drawing 3 (a)]. Although diffusion of an impurity hardly breaks out in SiC as stated previously, the depth in which an impurity range is formed is controllable by accommodation of acceleration voltage. For example, p+ The embedding field 42 is made by the layer with a thickness of 0.5 micrometers at focusing on a depth of 0.8 micrometers by having made acceleration voltage high with 400keV(s), and n about 0.5-micrometer drift region 41b is left behind on it. p gate field 44 and n+ The depth of the source field 43 is about 0.2 micrometers.
[0038] To a front face, it is SiO2 by the CVD method. The film 2 is deposited [this drawing (b)]. It is n+ at RIE form the fourth mask M4 by the photolithography, and using the mixed gas of carbon tetrafluoride (CF4) and oxygen (O2). Crevice 47a which arrives at p+ embedding field 42 from the front face of the source field 43 is formed [this drawing (c)]. It is SiO2 at a photolithography. After forming opening for contact in the film 2 Pattern formation of the aluminium alloy film is vapor-deposited and carried out, and it considers as the source electrode 47 and the gate electrode 46., n+ A drain electrode is prepared also in the rear face of a substrate, and a process is completed [this drawing (d)].
[0039] By taking the above manufacture approaches, it was able to consider as the high proof-pressure SiC vertical mold JFET of drawing 1 . SiCJFET of an example 1 -- a part of first mask -- the edge of M1b -- n+ the source field 43 specifies -- having -- a part of first mask -- p gate field 44 is prescribed by another edge of M1b, and another partial M1a of the first mask. By partial M1a with the first still more nearly another mask, it is p+. The edge of the embedding field 42 is specified. Thus, since the impurity range is prescribed by only the first mask M1, each has consistency and the problem of the ununiformity by mask alignment, such as a location gap, cannot arise. After the pattern formation of the first mask M1, the advantage that the dimension of each impurity range can be checked is also.
[0040] Although the control is very important on application since the die length of a channel field is a main parameter which determines the property of MOSFET, in SiCJFET of this example 1, the n channel field 50 of the lower part of p gate field 44 serves as channel length substantially, channel length is formed with a precision short and sufficient to homogeneity, and the stable property and the high yield are obtained. The on resistance of JFET of 1500V class made as an experiment showed 15m ohm-cm -2 and a low value.
[0041] Moreover, p+ The embedding field 42 was formed by the ion implantation with high acceleration voltage, the junction depth was written deeply, and high pressure-proofing beyond 1500V has been realized easily. By having been added like N ion grouting for high-impurity-concentration control to the surface layer of n drift layer 41b, the threshold voltage of MOSFET can be controlled and it can also be referred to as FET of no MARIOFU.
[0042] Some deformation is also considered as the manufacture approach. For example, n+ Reverse is sufficient as the sequence of the ion implantation for forming the source field 43 and p gate field 44. Moreover, the ion implantation for high-impurity-concentration control of the n channel field 50 may be performed first. If it will carry out at low temperature more instead of an elevated temperature which calls an ion implantation 1000 degrees C, the selection width of face of a mask ingredient can extend.
[0043] [Example 2] drawing 4 is the fragmentary sectional view of SiCJFET concerning the second example of this invention. This is the modification of the example 1 of drawing 1 . A

crevice is not formed in a SiC substrate front face in this example, but it is p+ to the surface layer of n drift layer 51b. p+ which arrives at the embedding field 52 Contact field 52a is formed and it is n+ to that front face. The source field 53 and the common source electrode 57 are formed.
[0044] n+ As a mask (it is equivalent to M2 of drawing 2 (b)) in the case of N ion implantation for source field 53 formation, it is n+. The mask which also specifies the outside of the source field 53 is used, still more nearly another mask is used, and it is p+. What is necessary is just to perform B ion implantation for contact field 52a formation. If it does in this way, a crevice cannot be formed but an electrode can be prepared in a substrate front face.
[0045] n+ There is instead of [no] in a part of first mask (it being equivalent to M1b of drawing 2 (b)) specifying the inside of the source field 53, and the die length of a channel field is the same as that of SiCJFET of an example 1, the n channel field 60 of the lower part of p gate field 44 has short uniform channel length, it is form with a sufficient precision, and the stable property and the high yield are obtain.
[0046] [Example 3] drawing 5 is the fragmentary sectional view of SiCJFET concerning the third example of this invention. This can also say it also as deformation of SiCJFET of drawing 1 . The point different from SiCJFET of drawing 1 is a point that the gate electrode 66 touches common to p gate field 64 and the front face of n drift layer 61b. Here, the gate electrode 66 chooses a SiC substrate and a metal which forms the Schottky barrier, for example, Ti, aluminum, Pt, etc.
[0047] At JFET of an example 1, as for p gate field 44, contact is taken only in the part which the gate electrode 46 contacts so that drawing 1 may show. In order to stop this contact resistance small, the touch area had to be enlarged and the magnitude of this contact aperture had restricted the minimum value of the die length of a channel. Since JFET of this example 3 improves this point and the gate electrode 66 touches not only p gate field 64 but the front face of n drift layer 61b, a large contact part can be taken and it becomes possible to design a channel field narrowly.
[0048] It also sets to JFET of this example 3, and is n+. It is the same that the property which a source field carries out self align to the surface layer of p base region, and is formed, and channel length was formed with a uniformly and sufficient precision like JFET of an example 1, and was stabilized is acquired with the sufficient yield. However, the gate electrodes 66 are a SiC substrate and the metal which forms the Schottky barrier, and are not necessarily the same metal as the source electrode 67. Or the gate electrode 66 may be made into a bilayer with the same metal as the metal and the source electrode 67 which carry out Schottky contact. About the process which manufactures this, it is almost almost the same as that of drawing 2 and 3, and explanation is omitted.
[0049] [Example 4] drawing 6 is the fragmentary sectional view of SiCMOSFET concerning the fourth example of this invention. n+ In the wafer with which the laminating of the n drift layer 71b was carried out by epitaxial growth on substrate 71a It is p+ from the front face of n drift layer 71b to a somewhat deep location. The embedding field 72 is formed and it is the p+. It is n+ to the surface layer of upper n drift layer 71b of the embedding field 72. Although the point that the source field 73 is formed is the same as an old example There is nothing and p gate field is p+. The upper part of the embedding field 72 is made into the n channel field 80, and the gate of metal-oxide-semiconductor structure is prepared on the front face.
[0050] That is, the gate electrode layer 76 which consists of a polycrystalline silicon layer through gate oxide 75 is formed on the front face of n drift layer 71b. 79 is an insulator layer of boron phosphorus silica glass (BPSG) which insulates the gate electrode layer 76 and the source electrode 77. n+ There is crevice 77a investigated from the front face of the source field 73, the

front face is met, and it is n+. The source field 73 and p+ The source electrode 77 which contacts common to a front face with the embedding field 72 is formed, and it is n+. The rear face of substrate 71a is contacted and the drain electrode 78 is formed. The dimension of main each part is almost the same as the value stated in the example 1. The thickness of gate oxide 75 is [the thickness of 1 micrometer and an insulator layer 79 of the thickness of 50nm and the gate electrode layer 76] 2 micrometers.

[0051] When this MOSFET is also called ACCUFET and impresses a forward electrical potential difference to the gate electrode layer 76, induction of the accumulation layer is carried out to the surface part of n drift layer 71b of gate electrode layer 76 directly under, and a current flows between the drain electrode 78 and the source electrode 77. Moreover, if a negative electrical potential difference is impressed to the gate electrode layer 76, the current between the drain electrode 78 and the source electrode 77 can be intercepted, and it has a switching function. The electrical potential difference between source drains is p+. It is possible for it to be impressed between the embedding field 72 and n drift layer 71b, and to hold a big electrical potential difference, and it has structure suitable for high pressure-proofing.

[0052] Drawing 7 (a) thru/or (e) and drawing 8 (a) thru/or (d) are the fragmentary sectional views of the order of a production process near the front face of SiCMOSFET of the example 4 of drawing 6 . A process is explained in order of below. n+ 4 H-SiC substrate which carried out the laminating of the n drift layer 71b of a phosphorus dope with epitaxial growth is prepared on substrate 71a. The high impurity concentration of n drift layer 71b, thickness, etc. are the same as an example 1, and good. On the front face of the n drift layer 71b, a polycrystal silicone film is deposited with a reduced pressure CVD method, a pattern is formed by the photolithography, and it considers as the first mask M1 [drawing 7 (a)]. The first mask M1 consists of each part of M1a of a center section, and M1b of both sides. It is the same as that of an example 1 that it is not necessary to be necessarily a polycrystal silicone film of the first mask M1.

[0053] It is SiO2 by the heat CVD method on the first mask M1 of a polycrystal silicone film. After depositing the film, forming a pattern by the photolithography and considering as the second mask M2, the ion used as n mold impurity, for example, N ion 4a, is poured into the field specified with the second mask M1 and M2 for a start [these] [this drawing (b)]. This is n+. It is for source field 73 formation, and acceleration voltage, a dose, etc. are the same as an example 1, and good. this second mask M2 -- not necessarily -- SiO2 it is not necessary to be -- although -- since it is required to remove leaving the first mask M1 at a next process, unlike the first mask M1, the ingredient which can perform alternative etching is chosen. Since the second mask M2 should just have an edge on the first mask M1, it is easy mask alignment. As an n mold impurity, P etc. is used other than N.

[0054] SiO2 the second membranous mask M2 -- removing -- a photolithography -- a part of first mask -- [this drawing (c)] which pours in the ion used as p mold impurity, for example, B ion 5a, after leaving M1a. This is p+. It is for embedding field 72 formation, and acceleration voltage is 400keV(s) and a dose is abbreviation 1x1015cm-2. Acceleration voltage was raised for forming a deep impurity range. As for p mold impurity, aluminum etc. is used other than B.

[0055] a part of first mask which it left -- M1a is removed and N ion 4a is poured in. [This drawing (d)]. This is for high-impurity-concentration control of the n channel field 80, acceleration voltage is 200keV(s) and a dose is abbreviation 1x1012cm-2. It is p+ by performing 1600 degrees C and heat treatment of 2 hours, and activating the poured-in impurity. The embedding field 72 and n+ Each field of the source field 73 and the n channel field 80 is formed [this drawing (e)].

[0056] SiO2 film which turns into gate oxide 75 by 1200 degrees C and thermal oxidation of 2 hours is formed in a front face, and about 1 micrometer of polycrystal silicone films 1 which serve as a gate electrode layer with a reduced pressure CVD method continuously is deposited [drawing 8 (a)]. It forms by thermal oxidation, and also gate oxide 75 can also form membranes by CVD. As an ingredient of the gate electrode layer 76, molybdenum (Mo) etc. is [other than polycrystalline silicon] usable.
[0057] A photoresist is applied, and after carrying out pattern formation of the polycrystal silicone film 1 by the photolithography and considering as the gate electrode layer 76, the insulator layers 79, such as boron phosphorus silica glass (BPSG), are deposited on a front face with a CVD method [this drawing (b)]. It is n+ at RIE form a pattern by the photolithography and using the mixed gas of carbon tetrafluoride (CF4) and oxygen (O2). The front face of the source field 73 to p+ Crevice 77a which arrives at the embedding field 72 is formed [this drawing (c)].
[0058] After forming opening for contact in an insulator layer 79 by the photolithography, pattern formation of the aluminium alloy is vapor-deposited and carried out, and it considers as the source electrode 77 and the gate electrode which is not illustrated. n+ A drain electrode is prepared also in the rear face of a substrate, and a process is completed [this drawing (d)]. MOSFET of this example 4 -- also setting -- a part of first mask -- the edge of M1b -- n+ The source field 73 is specified and the edge of p+ embedding field 72 is prescribed by partial M1a with the first another mask. Thus, since the impurity range is prescribed by only the first mask M1, each has consistency and the problem of the ununiformity by mask alignment, such as a location gap, cannot arise.
[0059] Therefore, like JFET of an example 1, about 1.5-micrometer channel length is realized with a uniformly and sufficient precision, and the stable property is acquired with the sufficient yield. After formation of the first mask 1, the advantage that the dimension of each impurity range can be checked is also. By being added like N ion grouting for high-impurity-concentration control to the surface layer of n drift layer 71b, and considering as the n channel field 80, the threshold voltage of MOSFET can be controlled and it can also be especially referred to as FET of no MARIOFU.
[0060] Moreover, since gate oxide 75 is formed on the SiC substrate at the plane, there is no problem of the stress of the electric field in the corner section of the gate oxide seen by MOSFET conventional trench type, and a raise in pressure-proofing is possible. Some deformation is also considered as the manufacture approach. For example, the ion implantation for high-impurity-concentration control of the n channel field 80 may be performed first, and reverse order is sufficient as formation with the second mask M2 and the third mask M3.
[0061] n+ In the case of N ion implantation for source field 73 formation, it is n+. The mask which specifies the outside of the source field 73 is used, still more nearly another mask is used, and it is p+. If B ion implantation for contact field 52a formation is performed, crevice 77a cannot be formed but an electrode can be prepared in a substrate front face. In that case The die length of a channel field is formed in homogeneity with a sufficient precision like SiCMOSFET of an example 4, and the stable property and the high yield are obtained.
[0062] [Example 5] drawing 9 is the fragmentary sectional view of SiCMOSFET concerning the fifth example of this invention. n+ It is p+ to a somewhat deep location from the front face of n drift layer 81b deposited with epitaxial growth on substrate 81a. The embedding field 82 is formed and it is p+. The p base region 82 is formed in the surface layer of upper n drift layer 81b of the embedding field 82, and it is n+ alternatively in the upper part. The source field 83 is

formed. And the part of the edge of the p base region 82 is n+. It is so characteristic that it keeps away from the source field 83 that the junction depth is shallow almost linearly. Moreover, it is p+ to a part deeper than the p base region 82 so that the p base region 82 may be overlapped in part. Contact field 82a is formed. n+ The upper part of the p base region 82 of a part in which the source field 83 is not formed is made into the n channel field 90, and the gate of the same metal-oxide-semiconductor structure as MOSFET of drawing 6 is prepared on it. That is, the gate electrode layer 86 which consists of a polycrystalline silicon layer through gate oxide 85 is formed. 89 is the insulator layer of BPSG which insulates a gate electrode layer and the source electrode 87. n+ From the front face of the source field 83, there is investigated crevice 87a and it is n+. The source field 83 and p+ It contacts common to a front face with the contact field 82, and the source electrode 87 is formed, and it is n+. The rear face of substrate 81a is contacted and the drain electrode 88 is formed.

[0063] Examples of the main dimensions are the following values. n+ For the high impurity concentration of substrate 41a, it of 1x1018cm in 350 micrometers in 3 and thickness and n drift layer 41b is 1x1016cm 10 micrometers in 3 and thickness. Spacing between 3 and a junction depth of 1.5 micrometers of 5x1016cm, and the p base region 82 of both sides of the highest high impurity concentration of the p base region 82 is about 6 micrometers. n+ The high impurity concentration of the source field 43 is 1x1019cm 3 and a junction depth of 0.2 micrometers, and width of face is about 5 micrometers and p+. The highest high impurity concentration of the contact field 82 is [the high impurity concentration of about 5 micrometers and the n channel field 90 of 3 and a junction depth of 2.0 micrometers of 1x1019cm, and width of face] 5x1015cm 3 and a junction depth of 0.5 micrometers. n+ Spacing between the edge of the source field 83 and the edge of the p base region 82 is about 2 micrometers. The depth of crevice 87a investigated from the front face is 0.7 micrometers, and width of face is about 3 micrometers. The pitch of the unit cell of drawing is about 30 micrometers. The thickness of gate oxide 85 is [the thickness of 1 micrometer and an insulator layer 89 of the thickness of 50nm and the gate electrode layer 86] 2 micrometers.

[0064] Drawing 10 (a) thru/or (e) and drawing 11 (a) thru/or (e) are the fragmentary sectional views of the order of a production process near the front face of SiCMOSFET of the example 5 of drawing 9 . A process is explained in order of below. First, n+ 4 H-SiC substrate which carried out the laminating of the n drift layer 81b of a phosphorus dope with epitaxial growth is prepared on a substrate. On the front face of n drift layer 81b, a polycrystal silicone film is deposited with a reduced pressure CVD method, a pattern is formed by the photolithography, and it considers as the first mask M1.

[0065] It is important especially in the case of this patterning to form the taper section 8 in the edge of the first mask M1 over 1-2 micrometers. This is because channel length is controlled by the include angle of the taper section 8 of the first mask M1 in the ion implantation for the next p base region formation. Therefore, this cone angle must be captured and decided to be a predetermined design. And this include angle is controllable by choosing the etching conditions at the time of etching the thin film of the first mask 1 by plasma etching etc. Or a loose taper will be obtained, if an ion implantation is carried out to the upper part of a thin film, the damage is given to it and it carries out only near the front face that it is easy to be etched. There is also the approach of controlling a taper angle by controlling the dose of the ion implantation in that case.

[0066] The ion, for example, boron (B) ion 5a, which serves as p mold impurity by using the first mask M1 as a mask is poured in [drawing 10 (a)]. 5b is poured-in B atom. This is for p base region 82 formation, acceleration voltage is 300keV(s) and a dose is abbreviation 1x1015cm-2.

Acceleration voltage was raised for forming a deep impurity range. In a field without the first mask M1, an impurity is poured in deeply, it becomes shallow almost linear gradually as thickness of the mask [first] M1 increases, and an impurity atom carries out distribution as shown in drawing. If thickness of the first mask M1 is made to some extent thin, an impurity impregnation field does not arrive at even a front face, but can be made into the field of an embedding mold. As for p mold impurity, aluminum etc. is used other than B. It is the same as that of an example 1 that it is not necessary to be necessarily a polycrystal silicone film of the first mask M1.

[0067] Next, the ion, for example, N ion 4a, which serves as n mold impurity by using the first same mask M1 as a mask is poured in [this drawing (b)]. 4b is poured-in n atom. This is for n+ source field 83 formation, and the 100keV(s) as an example 1 with the same acceleration voltage etc. and a dose are good at abbreviation 5x1015cm-2. In the field which does not have the first mask M1 in this case, either, an impurity is poured in deeply, if the first mask M1 becomes thick, it will become shallow gradually, and an impurity atom carries out distribution as shown in drawing. However, since acceleration voltage is made low, the field poured in differs from the impregnation field of B ion. If the include angle of the taper section 8 is the same, spacing of the impregnation field of p mold impurity and the impregnation field of n mold impurity will become fixed.

[0068] It is SiO2 by the heat CVD method on the first mask M1 of a polycrystal silicone film. The film 2 is deposited [this drawing (c)]. After forming a sidewall 9 in the side of ** and the taper section 8 of the first mask M1 carrying out overall etching by RIE, the ion used as p mold impurity, for example, B ion 5a, is poured into the field specified by these first masks M1 and the sidewall 9 [this drawing (d)]. This is high-concentration p+. It is for contact field 84 formation, and acceleration voltage, 400keV, and a dose are abbreviation 1x1015cm-2. As a p mold impurity, aluminum etc. is used other than B.

[0069] After removing the first mask M1 and a sidewall 9, N ion 4a is poured into the whole surface. [This drawing (e)]. This is for high-impurity-concentration control of the n channel field 90, acceleration voltage is 200keV(s) and a dose is abbreviation 1x1012cm-2. Thereby, a threshold is controllable. Each field is formed by performing 1600 degrees C and heat treatment of 2 hours, and activating the poured-in impurity [drawing 11 (a)]. Thus, p base region 82sn+ The source field 83 can be shifted and formed.

[0070] Heat SiO2 with a thickness of 50nm it is thin to gate oxide 85 on a front face with 1200 degrees C and thermal oxidation of 2 hours The film 6 is formed, and about 1 micrometer of polycrystal silicone films 1 is continuously deposited with a reduced pressure CVD method [this drawing (b)]. It forms by thermal oxidation, and also gate oxide 85 can also form membranes by CVD. After applying a photoresist, carrying out pattern formation of the polycrystal silicone film 1 by the photolithography and considering as the gate electrode layer 86, with a CVD method, the insulator layers 89, such as boron phosphorus silica glass (BPSG), are deposited on a front face, and a pattern is formed in it by the photolithography [this drawing (c)].

[0071] At RIE using the mixed gas of carbon tetrafluoride (CF4) and oxygen (O2), it is p+ from the front face of n+ source field 83. Crevice 87a which reaches contact field 82a is formed [this drawing (d)]. After forming opening for contact in an insulator layer 89 by the photolithography, pattern formation of the aluminium alloy is vapor-deposited and carried out, and it considers as the source electrode 87 and the gate electrode which is not illustrated [this drawing (e)]. n+ A drain electrode is prepared also in the rear face of a substrate, and a process is completed.

[0072] In MOSFET of this example 5, the edge of n+ source field 83 and the p base region 82 is

prescribed by by making the edge of the first mask 1 into the shape of a taper, and changing the acceleration voltage in the case of impregnation of p mold impurity and n mold impurity. That is, the channel length who is spacing between both is prescribed by the taper section 8 of the first mask M1. Thus, since the impurity range is prescribed by only the first mask, both have consistency and the problem of the ununiformity by mask alignment, such as a location gap, does not occur.

[0073] Therefore, channel length is formed in homogeneity with a sufficient precision, and the stable property is acquired with the sufficient yield. Moreover, if the include angle of the taper section 8 of the first mask M1 is changed, both spacing, i.e., the die length of a channel field, can be controlled freely, and the balance of on resistance and pressure-proofing will also tend to take it. After formation of the first mask 1, the advantage that the dimension of each impurity range can be checked is also.

[0074] By having been added like N ion grouting for high-impurity-concentration control to the surface layer of n drift layer 81b, the threshold voltage of MOSFET can be controlled and it can also be especially referred to as FET of no MARIOFU. Some deformation is also considered as the manufacture approach. For example, the ion implantation for high-impurity-concentration control of the n channel field 90 may be performed first. Moreover, impregnation and n+ of B ion for the p base region 82 Reverse is sufficient as the order of impregnation of N ion for source field 83 formation. A sidewall field is formed first and it is p+. The ion implantation for contact field 84 formation may be performed.

[0075] Since gate oxide 85 is formed on the SiC substrate also in this example at the plane, there is no problem of the stress of the electric field in the gate oxide corner section seen by MOSFET conventional trench type, and a raise in pressure-proofing is possible. Moreover, at this example, it is p+. It is n+, although contact field 82a was embedded and being considered as the field of a mold. In the case of N ion implantation for source field 83 formation, it is n+. The mask which specifies the outside of the source field 83 is used, and it is p+. If contact field 82a is made to arrive at even a front face by multiplex impregnation, the source electrode 87 can be formed in a substrate front face, and there will be no need of forming crevice 87a.

[0076] [Example 6] drawing 12 (a) thru/or (e) are the fragmentary sectional views near the front face of the order of a production process for explaining the another manufacture approach of the almost same SiCMOSFET as SiCMOSFET of drawing 9 . A process is explained in order of below. First, n+ 4 H-SiC substrate which carried out the laminating of the n drift layer 91b of a phosphorus dope with epitaxial growth is prepared on a substrate. The high impurity concentration of n drift layer 91b, thickness, etc. are the same as an example 1, and good. On the front face of the n drift layer 91b, it is SiO2 with a thickness of about 2 micrometers by the plasma-CVD method. The film 2 is deposited, a pattern is formed by the photolithography, and it considers as the third mask M3.

[0077] The ion, for example, B ion 5a, which serves as p mold impurity by using the third mask M3 as a mask is poured in [drawing 12 (a)]. 5b is poured-in B atom. This is high-concentration p+. It is for contact field 94 formation, and acceleration voltage, 400keV, and a dose are abbreviation 1x1015cm-2. As a p mold impurity, aluminum etc. is used other than B.

[0078] Next, CF4+H2 It considers as the first mask M1 which carried out etchback of the third mask M3, and made the edge the shape of a taper over 1-2 micrometers by plasma etching using gas [this drawing (b)]. At this time, the whole thickness also becomes thin and thickness is set to about 1 micrometer. In the ion implantation for the next p base region formation, a channel is controlled by the cone angle of the edge of the first mask by this like the time of SiCMOSFET of

an example 5.
[0079] The ion, for example, B ion 5a, which serves as p mold impurity by using as a mask the first mask M1 which made the edge the shape of a taper is poured in [this drawing (c)]. This is for p base region 92 formation, acceleration voltage is 300keV(s) and a dose is abbreviation 1x1015cm-2. In a field without the first mask M1, an impurity is poured in deeply, it becomes shallow gradually as thickness of the mask [first] M1 increases, and an impurity atom carries out distribution as shown in drawing.
[0080] Next, the ion, for example, N ion 4a, which serves as n mold impurity by using as a mask the first mask M1 which made the same edge the shape of a taper is poured in [this drawing (d)]. This is n+. It is for source field 93 formation, and acceleration voltage is 100keV(s) and a dose is abbreviation 5x1015cm-2. Since acceleration voltage is made low, the field poured in differs from the impregnation field of p mold impurity.
[0081] After removing the first mask M1, N ion 4a is poured into the whole surface. [This drawing (e)]. This is for high-impurity-concentration control of the n channel field of the surface layer of n drift layer 91b, acceleration voltage is 200keV(s) and a dose is abbreviation 1x1012cm-2. Thereby, a threshold is controllable. After this, activation of the impurity poured in after drawing 10 (a), formation of an electrode, etc. are performed.
[0082] Since back dirty [of the third mask M3] was carried out and it considered as the first mask M1 when taking this approach, it is not necessary to form a mask ingredient anew. And since the include angle of the taper section also becomes homogeneity and spacing of the p base region 92 and n source field 93 is specified, both have consistency and the problem of the ununiformity by mask alignment, such as a location gap, cannot arise. And channel length is formed in homogeneity with a sufficient precision, and the stable property is acquired with the sufficient yield.
[0083] Some deformation is also considered as the manufacture approach. For example, a reverse order is sufficient as impregnation [drawing 12 (c)] of p mold impurity ion for p base region formation, and impregnation [drawing 12 (d)] of n mold impurity ion for n source field formation, and the ion implantation for high-impurity-concentration control of an n channel field [drawing 12 (e)] may be performed first.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The fragmentary sectional view of MOSFET of the first example of this invention
[Drawing 2] (a) - (f) is the fragmentary sectional view of the order of a process for explaining the manufacture approach of JFET of an example 1.
[Drawing 3] (a) - (d) is the fragmentary sectional view of the order of a process of JFET of the example 1 following drawing 2 (f).
[Drawing 4] The fragmentary sectional view of JFET of an example 2
[Drawing 5] The fragmentary sectional view of JFET of an example 3
[Drawing 6] The fragmentary sectional view of MOSFET of an example 4
[Drawing 7] (a) - (e) is the fragmentary sectional view of the order of a process for explaining the manufacture approach of MOSFET of an example 4.
[Drawing 8] (a) - (d) is the fragmentary sectional view of the order of a process of MOSFET of the example 3 following drawing 7 (e).
[Drawing 9] The fragmentary sectional view of MOSFET of an example 5
[Drawing 10] (a) - (e) is the fragmentary sectional view of the order of a process for explaining the manufacture approach of MOSFET of an example 5.
[Drawing 11] (a) - (e) is the fragmentary sectional view of the order of a process of MOSFET of the example 5 following drawing 10 (e).
[Drawing 12] (a) - (e) is the fragmentary sectional view of the order of a process for explaining the manufacture approach of MOSFET of an example 6.
[Drawing 13] The fragmentary sectional view of the conventional JFET
[Drawing 14] The fragmentary sectional view of the conventional MOSFET
[Drawing 15] The fragmentary sectional view of another conventional MOSFET
[Description of Notations]
M1, M1a, M1b The first mask
M2 The second mask
M3 The third mask
1 Polycrystal Silicone Film
2 SiO2 Film
3 Insulator Layer
4a Nitrogen ion
4b Nitrogen atom
5a Boron ion
5b Boron atom
6 Thermal Oxidation Film
7 Crevice

8 Taper Section
9 Sidewall
10 P Mold Substrate
11a n+ Drain field
11b, 21b, 31b, 41b, 51b, 61b, 71b, 81b n drift layer
13, 23, 33, 43, 53, 63, 73, 83 n+ Source field
14, 44, 54, 64 p gate field
16, 46, 66 Gate electrode
17, 27, 37, 47, 57, 67, 77, 87 Source electrode
18, 28, 38, 78, 88 Drain electrode
19, 39, 49, 59, 69, 79, 89 Insulator layer
20, 30, 40, 50, 60, 70, 80, 90 Channel field
21a, 31a, 41a, 71a, 81a n+ Drain layer
22, 42, 52, 72 p+ Embedding field
25, 35, 75, 85 Gate oxide
26, 36, 76, 86 Gate electrode layer
32 82 p base region
37a, 47a, 77a, 87a Crevice
52a, 82a p+ Contact field

[Translation done.]